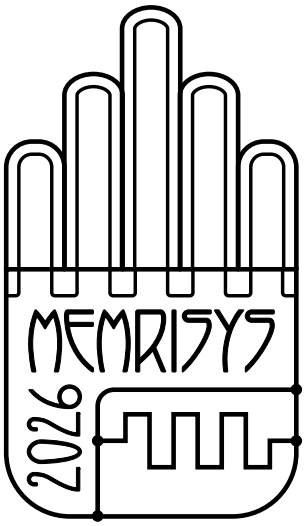


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Talks

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Electrochemical Ionic Synapses for Energy-Efficient Brain-Inspired Computing

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In this talk, I will share our work on the ionic electrochemical synapses, whose electronic conductivity we control deterministically by electrochemical insertion/extraction of dopant ions into/out of the channel layer. This work is motivated by the need to enable significant reductions in the energy consumption of computing, and is inspired by the ionic processes in the brain. Proton as the working ion in our research presents with very low energy consumption, on par with biological synapses in the brain. Our modeling results indicate the desirable material properties, such as ion conductivity and interface charge transfer kinetics, that we must achieve for fast (ns), low energy (< fJ) and low voltage (<1V) performance of these devices. Importantly, the target material is a mixed proton-electron conductor, whose electronic conductivity depends on the proton concentration through doping and phase change effects. The candidate materials are a spectrum of intercalation oxides as well as 2D van der Waals materials. We have assessed the electron polaron and proton mobilities in these systems, to understand the conductivity modulation mechanisms, and down-select most promising materials. In addition, the conductance change in these electrochemical devices depends non-linearly on the gate voltage, due to field-enhanced ion migration in the electrolyte, and charge transfer kinetics at the electrolyte-channel interface. We are leveraging these intrinsic nonlinearities to emulate bio-realistic learning rules deduced from neuroscience studies, such as spike timing dependence of plasticity and Hebbian learning rules. Our findings provide pathways towards brain-inspired hardware that has high yield and consistency and uses significantly lesser energy as compared to current computing architectures.

Mitigating Long Read Latencies in Gradual Switching Valence Change Memories through Barrier Engineering

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The growing demand for energy-efficient AI hardware has stimulated considerable interest in computing-in-memory (CIM) and neuromorphic architectures. In these systems, memristive devices enable analog vector–matrix multiplication directly within memory arrays and can emulate biological synaptic plasticity [1–3]. Among the available technologies, valence change memories (VCMs) are particularly promising due to their CMOS compatibility, scalability, and multilevel switching capabilities [4,5]. While abrupt-switching VCMs have already been successfully integrated into foundry technologies for memory applications [6], the deployment of gradual analog VCM devices for large-scale AI hardware remains limited by unresolved challenges at the device, circuit, and system levels [7].

One of the most widely recognized bottlenecks in CIM hardware is the latency and energy overhead associated with peripheral readout circuitry, particularly analog-to-digital converters (ADCs) [8-10]. Consequently, research efforts have focused primarily on reducing circuit-level readout costs, while the intrinsic read dynamics of individual memristive devices have received comparatively little attention. This emphasis is based on the assumption that device-level read processes are substantially faster than peripheral operations and therefore have negligible impact on overall system performance [8-10]. While this assumption is well justified for abrupt filamentary switching devices [4,5], gradual-switching VCMs are routinely operated with read pulses ranging from microseconds to multiple milliseconds to achieve stable analog readouts [11–13]. This raises a fundamental question: does intrinsic device read latency itself constitute a previously overlooked bottleneck for analog memristive computing?

Here, we first demonstrate that gradual-switching VCMs indeed exhibit intrinsic read latencies extending into the millisecond regime, revealing a limitation that can directly limit the performance of next-generation CIM hardware. Notably, these slow read dynamics are closely linked to the pronounced zero-crossing behavior frequently observed in the current–voltage characteristics of analog VCM devices, a long-standing phenomenon whose physical origin has remained unresolved [14].

To uncover the underlying mechanism, we develop a physical model based on trap-mediated electron exchange processes and show that the characteristic read latency is governed by trap–band electron exchange rates. Guided by this understanding, we employ targeted band-structure engineering of the device heterostructure and demonstrate a substantial reduction in read latency. Furthermore, we establish a power-law dependence between read speed and device current, revealing a favorable scaling trend: as device dimensions shrink and current densities increase, intrinsic readout becomes faster. This result indicates that a fundamental limitation can be mitigated through continued technology scaling.

At the same time, our findings expose an important trade-off for analog VCM design. High-resistance devices are often favored for large-scale array integration because they reduce power consumption and mitigate line-resistance effects [15]. However, the observed current dependence implies that these operating regimes are also most susceptible to long intrinsic read latencies. Intrinsic readout speed must therefore be considered alongside energy efficiency when optimizing memristive devices for large-scale CIM systems.

Overall, our results identify intrinsic read latency as a critical and previously overlooked limitation for analog memristive computing and provide a physics-based pathway toward faster and more scalable CIM hardware.

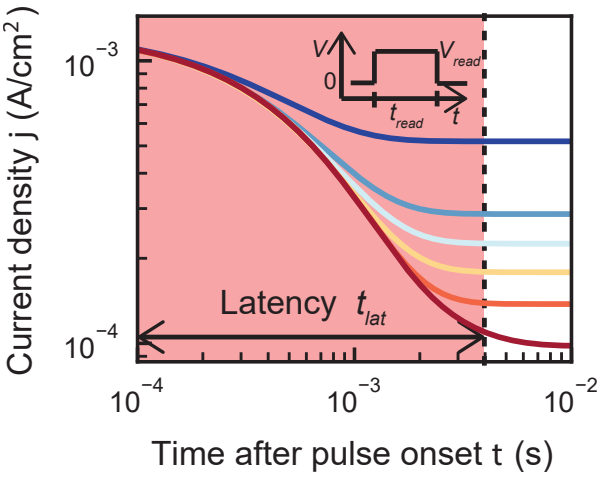


Figure 1. Comparison of pulsed readout transients for different ionic states in amorphous $SrTiO_3$-based memristive devices. The individual current levels can only be discriminated after a characteristic delay in the millisecond regime, demonstrating that the devices are limited by intrinsic read latency.

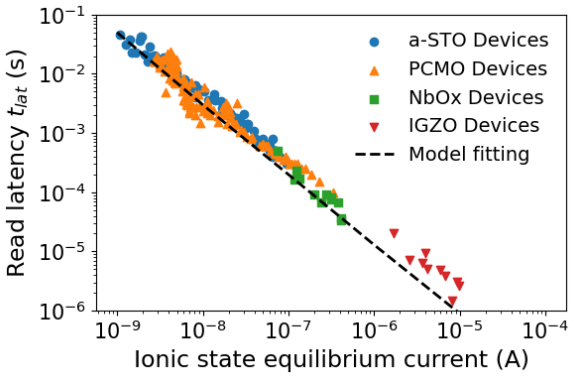


Figure 2. Read latency vs ionic-state equilibrium current for different gradual-switching VCM devices and ionic states. The dashed line shows the prediction of the trap-mediated readout model, which closely reproduces the experimentally observed power-law dependence.

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Aqueous proton-permeable graphene chemimemristor for robust electrochemical reservoir computing

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Inspired by ion-mediated information processing in the human brain, electrochemical memristive devices that emulate chemical synaptic behavior for neuromorphic computing in aqueous environments at low voltages have attracted significant attention. In this work, we report a proton-permeable graphene-based aqueous chemimemristor for spatiotemporal information processing. The device operates at an low programming voltage of 0.4 V with a reading voltage of -2 mV, which regulates interfacial proton transport to induce a electrochemical memristive effect. Benefiting from its non-destructive conductance modulation mechanism, the chemimemristor exhibits exceptional durability, with less than 1.4% fluctuation in dynamic range over 10,000 potentiation-depression cycles. This robust performance enables the establishment of an electrochemical reservoir computing (EC-RC) framework for dynamic frame recognition and speech recognition. Our work highlights the potential of aqueous memristive devices for advanced neuromorphic computation in water-based and biointegrated technologies.

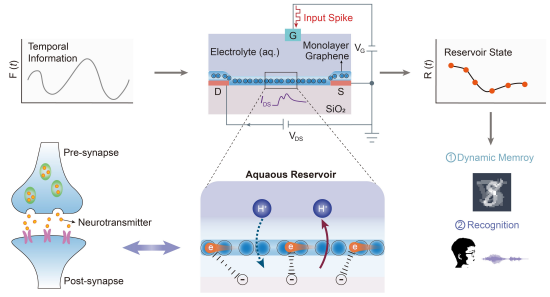


Figure 1. Our chemimemristor employs monolayer graphene as a tunable conductance channel and a NaCl water solution as the gate electrolyte. The migration of protons in an aqueous environment determining the conductance of graphene, is analogous to that of biological synapses, which enables effective time-series information processing.

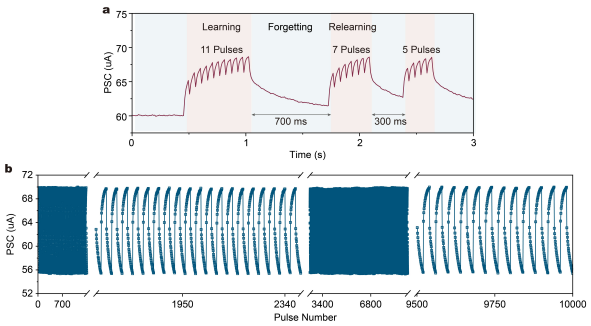


Figure 2. (a) Simulating the biological learning-forgetting-relearning process. (b) Endurance measurements under cyclic voltage pulses (20 pulses of VGS = -0.4 V, 20 pulses of VGS of 0.4 V. The pulse duration is 30 ms). Total pulses number is 10 000 in 250 cycles. VDS = -2 mV.

Multifunctional MoOx-based Volatile Memristor with Tunable Relaxation Dynamics Enabling Artificial Nociception and Neuromorphic Computing

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The rapid advancement of neuromorphic computing has driven a paradigm shift toward energy-efficient systems capable of emulating the parallel and adaptive functionalities of the human brain. Among emerging neuromorphic devices, volatile memristors garner significant attention owing to their spatiotemporal processing capabilities.[1,2] However, establishing a correlation between their intrinsic relaxation dynamics and diverse neuromorphic functionalities, including artificial nociception, synaptic plasticity, and neuromorphic computing, remains a challenge. Herein, a multifunctional volatile MoOx memristor (Au/Ti/MoOx/TiN) with a second-order relaxation dynamics is demonstrated, enabling the seamless integration of neuromorphic processing and computing within a single device. The fabricated memristor exhibits forming-free, non-filamentary switching with volatile behavior, characterized by well-defined second-order current relaxation upon bias removal. Mechanistic analysis reveals that the memristive behavior arises from the interplay between charge trapping/detrapping and oxygen-ion migration. Leveraging these intrinsic dynamics, the device showcases nociceptive functionality, including threshold activation, relaxation, no-adaptation, and sensitization, thereby recapitulating key features of biological pain perception. Analog synaptic plasticity is achieved via gradual conductance modulation, producing potentiation and depression behaviors that emulate biological synapses and support learning and forgetting behavior. The coexistence of nonlinearity and short-term memory is subsequently exploited for reservoir computing, achieving 98% accuracy in handwritten digit recognition. Finally, a proof-of-concept mechano-nociceptor and Morse code are implemented by integrating the memristor with a force-sensing resistor, enabling it to respond to mechanical stimuli.

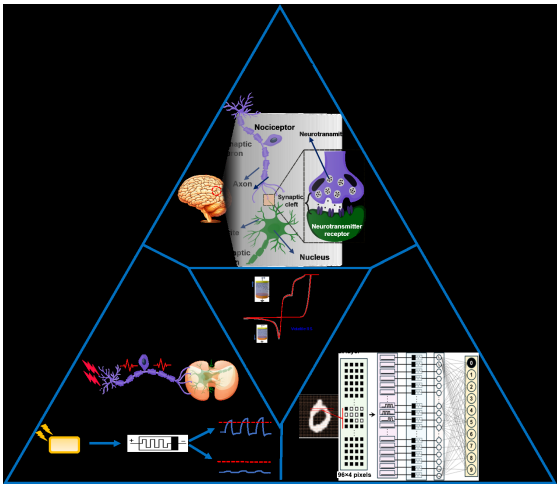


Figure 1. Volatile MoOx Memristor for Artificial Intelligent Applications

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Bidirectional Analogue Conductance Modulation in Wafer-Scale Ag/SnOx Electrochemical Metallisation Memristors

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Tin oxide exists across a range of oxygen stoichiometries, from the p-type SnO phase to the n-type SnO_2 end-member, and this tunability makes sub-stoichiometric SnOx an interesting candidate for resistive switching. Despite this, analogue synaptic behaviour in electrochemical metallisation (ECM) memristors based on Ag/SnOx/TiN stacks has received little attention compared with valence-change devices [1,2]. Here we report bidirectional pulse-addressable analogue conductance modulation in a non-volatile Ag/SnOx ECM device, fabricated within a systematic 2×2 process matrix on a single 6-inch silicon wafer using a fully CMOS-compatible stack.

The device structure — Ag (30 nm) / SnOx (35 nm) / TiN (60 nm) was realised across two reactive sputtering conditions (SnOx 2020 and SnOx 2010, corresponding to distinct Ar/O_2 flow ratios) and two top-electrode designs (Ag-only and Ag/Ti with a 3 nm Ti interlayer), enabling controlled on-wafer comparison of all four configurations. Breakdown characterisation of 55×55 μm^2 devices shows that SnOx 2020 conditions yield more controlled dielectric breakdown than SnOx 2010. Introducing a Ti interlayer severely degrades Ag conductive-bridge formation regardless of oxide condition, producing abrupt, poorly reproducible switching events; this is attributed to Ti-mediated suppression of Ag ion injection at the top electrode interface.

DC current–voltage characterisation across all four configurations confirms bipolar resistive switching with a –Forming/+Reset/–Set polarity sequence (Fig. 1). The SnOx 2020/Ag-only configuration is distinguished by tight cycle-to-cycle reproducibility, a well-defined self-limiting low-resistance state near 10^{-4} A, and stable non-volatile retention between switching events. The Ag/Ti variants show broader distributions consistent with disrupted filament nucleation, while SnOx 2010/Ag devices exhibit greater switching variability, plausibly reflecting less uniform oxide composition under higher oxygen-deficient sputtering. An HRS/LRS ratio exceeding 10^2 at 0.2 V read bias confirms a well-resolved switching window. These characteristics collectively motivated selection of SnOx 2020/Ag-only for synaptic characterisation.Pulse-driven measurements reveal bidirectional analogue conductance modulation. Negative pulses (–3 V, 750 µs) reduce conductance monotonically from ≈440 µS to ≈180 µS over 500 pulses, mimicking synaptic depression, while subsequent positive pulses (+2.7 V, 500 µs) restore conductance gradually to ≈260 µS over 1000 pulses, mimicking potentiation (Fig. 2). The absence of abrupt transitions throughout 1500 programming events is consistent with incremental modulation of the Ag conductive bridge [3,4], and positions SnOx as a scalable switching medium for analogue neuromorphic applications.

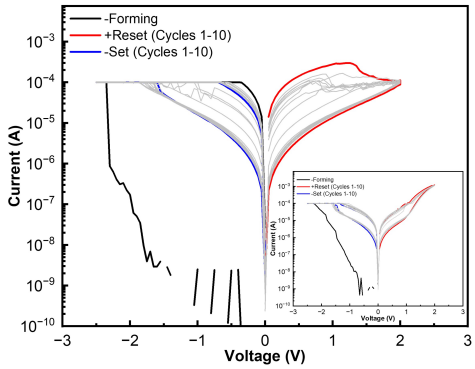


Figure 1. DC I–V characteristics of Ag/SnOx 2020 (main) and Ag/SnOx 2010 (inset) memristors (55×55 μm^2). Forming sweep (black), ten +Reset (red, cycle 1; grey, cycles 2–10) and –Set (blue, cycle 1; grey, cycles 2–10) cycles are shown for each device.

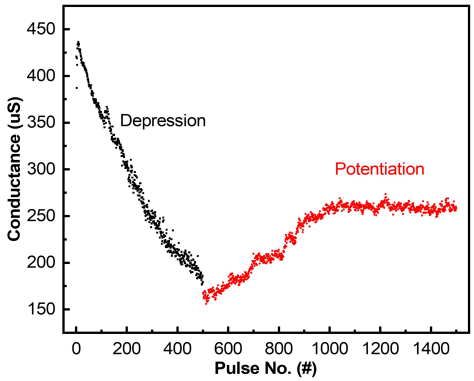


Figure 2. Bidirectional conductance modulation of an Ag/SnOx 2020 memristor (55×55 μm^2). Depression (black, 500 pulses at −3 V, 750 μs) and potentiation (red, 1000 pulses at +2.7 V, 500 μs) are read at 0.2 V.

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Temporal Evolution of Programmed Conductance in IGZO/HfO_2 Electrochemical Random-Access Memory

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Electrochemical random-access memories (ECRAMs) are commonly characterized using conductance values measured immediately after programming pulses. However, in barrier-confined ionic devices, the measured conductance may not directly represent the retained memory state because non-equilibrium ionic and interfacial processes continue after pulse termination. The temporal evolution of conductance in IGZO/HfO_2-based ECRAM devices is investigated using pulse programming and time-resolved read measurements. The measured conductance is decomposed into an instantaneous programmed component, a fast relaxation component, a slower vacancy-redistribution component, and a retained baseline state. Time- resolved measurements reveal that the apparent conductance continuously evolves after programming and cannot be described by a single relaxation process. Instead, at least two effective time constants are required to capture the observed evolution of conductance. Length- and amplitude-dependent measurements indicate that the transient and retained conductance components originate from distinct stages of oxygen-vacancy transport and relaxation. The proposed temporal decomposition consistently explains read-window-dependent conductance values, discrepancies between pulse-programmed and quasi-static measurements, and history-dependent conductance recovery observed during repeated programming cycles. These results demonstrate that the apparent conductance of oxide ECRAM devices depends strongly on the observation window following programming and should not be regarded as a single fixed state variable. The proposed framework provides a physically consistent method for separating transient relaxation effects from retained ionic states and offers practical guidelines for the characterization and optimization of analog ionic memory devices.

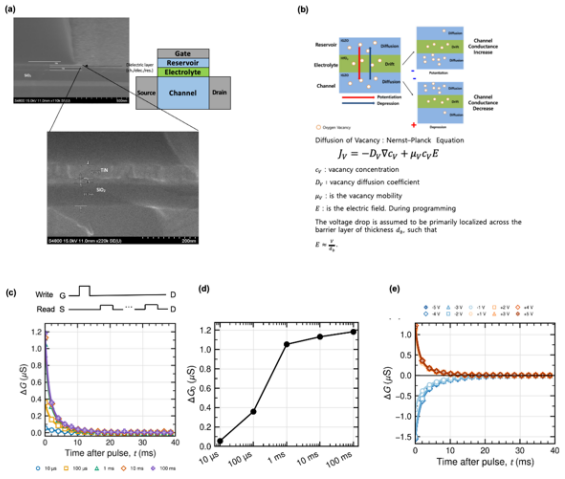


Figure 1. (a) Cross-sectional SEM images. (b) Device structure and proposed oxygen-vacancy transport mechanism. (c) Conductance relaxation after programming for different pulse widths. (d) Extracted ΔG0 as a function of pulse width. (e) Relaxation behavior after potentiation and depression operations.

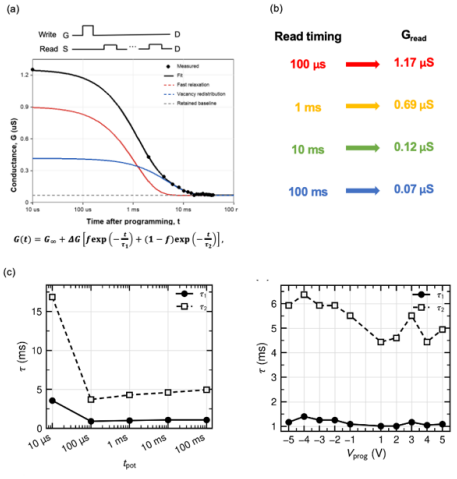


Figure 2. (a) Temporal evolution of programmed conductance following a write pulse. (b) Dependence of the measured conductance on the read timing. (c) Pulse-width dependence of the extracted relaxation time constants. (d) Programming-voltage dependence of the extracted relaxation time constants.

Talks

Edge Computing

Development of Emerging Memory Devices and Their Applications for Edge Computing

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Artificial intelligence (AI) will enable machines to think and solve complex tasks in ways similar to human beings. In recent years, artificial neural networks have significantly improved recognition and classification accuracy. However, state-of-the-art deep-learning algorithms require large network models with multiple layers, posing significant challenges for complementary metal-oxide-semiconductor (CMOS) implementation due to the difficulty of integrating computation, memory, and communication in large-scale networks.

As an alternative hardware platform, emerging memories have been proposed for weight storage and fast, low-power parallel neural computing. In this talk, Prof. Choi will present recent research results from systematic studies on two-terminal and three-terminal emerging memories. He will discuss approaches to achieving highly reliable artificial memories for neuromorphic computing, which may serve as a key step toward post-von Neumann computing. In addition, he will introduce applications of developed high-density memory architectures, highlighting the potential of emerging memory/computing device-based networks for efficient data processing and solving real-world problems. He will also discuss his recent work on phase-change memory that can operate in harsh environments. Finally, he will address the role of emerging memories in the era of data deluge.

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Energy-efficient uncertainty quantification via gate-tunable 1A1M synaptic array for Bayesian neural network

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Understanding and handling the potential uncertainty inherently existing in artificial intelligence (AI) technology are essential for adverting serious safety incidents and predictive failure that can profoundly affect human life. Furthermore, it is imperative to clearly acknowledge the limitations and intrinsic uncertainties of AI to effectively and safely collaborate between humans and AI for a particular task. To address these issues, uncertainty quantification techniques that assess potential scenarios and measure their objective probabilities have become increasingly vital. As a potential neural network for dealing with uncertainty in parameters, Bayesian neural networks (BNNs) based on Bayesian statistics have been suggested [1]. The BNNs are known to allow for the derivation of uncertainty by integrating new knowledge with prior knowledge and previous data using stochastic parameters. However, BNNs require advanced sampling techniques and multiple inference processes, thus necessitating novel devices capable of efficiently performing these suitable computations. Here, we present a three-terminal 1A1M synaptic device that integrates an IGZO active parameter modulator with a SiOx memristor, enabling both deterministic and probabilistic operations within a single structure. By controlling the gate voltage (0.4–5.5 V), the device independently modulates the mean (μ) and standard deviation (σ) of conductance, producing noise-enhanced and flexible synaptic weights. The fabricated 32 x 32 1A1M array demonstrated up to 20 conductance states with stable operation over 3,000 cycles, and when applied to a Hybrid Bayesian Convolutional Neural Network (HBCNN), it achieved 88.8 % accuracy, 0.93 AUROC for OOD detection, and 489× lower energy consumption compared to GPU-based systems, establishing it as a scalable hardware platform for uncertainty-aware AI.

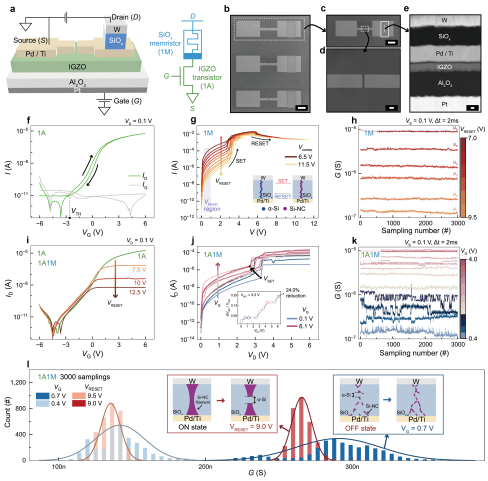


Figure 1. Monolithic 1A1M architecture and gate-tunable switching dynamics. a, Schematic and equivalent circuit of the one active parameter modulator–one memristor (1A1M) cell, featuring a vertical integration of a SiOx memristor (1M) onto an IGZO transistor (1A). b-e, Physical characterization. Top-view SEM images showing the device layout (b) and the IGZO channel region (c, d). Cross-sectional HR-TEM image (e) confirming the robust vertical stack with a shared Pd/Ti intermediate electrode. Scale bars: 100 µm (b, c), 10 µm (d), and 10 nm (e). f, Transfer ID–VG curves of the standalone 1A transistor exhibiting typical n-type behavior with low gate leakage current. g, Unipolar I–V switching characteristic of the standalone 1M device. Insets: Schematic of the filamentary switching mechanism involving the Si-NC and a-Si phases. h, Conductance evolution of the standalone 1M over 3,000 sampling cycles, demonstrating inherently deterministic behavior with negligible variation. i, Transfer curves of the integrated 1A1M cell measured after programming the 1M to different resistance states, confirming successful series coupling. j, Output characteristics (ID–VD) under varying VG. The inset shows the systematic reduction of the VSET voltage (ΔVSET/VSET, up to 24 %) as a function of VG, indicating that the 1A acts as an active parameter modulator. k, Real-time conductance evolution of the 1A1M cell under different VG, showing a transition from high-fluctuation probabilistic states (low VG, blue) to stable deterministic states (high VG, red). l, Statistical comparison of G histograms. The VRESET-modulation mode (red) yields sharp, deterministic distributions, whereas the low-VG modulation mode (blue) generates broad and probabilistic distributions suitable for Bayesian inference. Insets illustrate the proposed physical mechanism: formation of a single dominant gap for deterministic behavior versus multi-filamentary partial crystallization for probabilistic behavior.

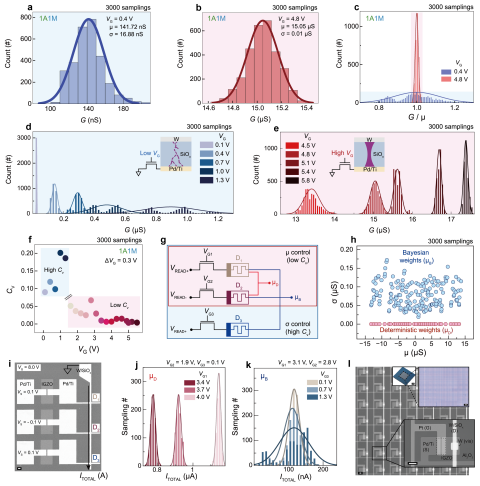


Figure 2. Operational library and array-level orthogonal control strategy. a-c, Gate-dependent stochasticity. Conductance histograms obtained from 3,000 sampling cycles contrasting the broad Gaussian distribution in the probabilistic mode (VG = 0.4 V) (a) with the sharp and confined distributions in the deterministic mode (VG = 4.8 V) (b). c, Comparison of normalized distribution (G/µ), visually highlighting the gate-tunable stochasticity. d, e, Evolution maps of conductance distributions across the full VG range, showing the transition from the low-VG probabilistic regime (d) to the high-VG deterministic regime (e). Insets depict the corresponding filamentary dynamics. f, Statistical evolution of the CV as a function of VG, revealing a clear bifurcation into high-CV (blue box) and low-CV (red box) operating regions. g, Circuit schematic of the parallel 1A1M array designed for decoupling µ and σ. The architecture comprises a deterministic µ-control block (D1 and D2 in red box) and a probabilistic σ-control block (D3 in blue box). h, Visualization of synthesized weight states in the 2D µ-σ parameter space. The µ-control block generates discrete deterministic points (red circles), which are expanded into a dense array of Bayesian weights (blue squares) by the σ-control block. i, Top-view SEM image of the fabricated 3 × 1 1A1M array consisting of two deterministic cells (D1, D2) and one probabilistic modulator cell (D3), which is used for validation. Scale bar: 10 µm. j, k, Experimental validation of orthogonal tuning. µ-tuning: Modulating the VG1 shifts the mean ITOTAL while maintaining negligible σ (j), σ-tuning: Modulating the low VG3 of the uncertainty injector (D3) significantly varies the σ without altering the ITOTAL (k). l, Optical and SEM images of the scalable 32 × 32 NOR-type 1A1M array. Each contains the full-chip, the optical image of entire array, a subsection SEM image, and a single-cell SEM image (Scale bars: 1 mm, 300 µm, 50 µm, and 50 µm, respectively).

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Memristor crossbar arrays as stateful outer-product engines for fully-parallel backpropagation weight updates

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Embodied artificial intelligence (EAI) requires intelligent agents capable of continuous, real-time learning within dynamic, unscripted environments. While memristor crossbar arrays (MXAs) have emerged as promising compute-in-memory (CIM) solutions to the von Neumann bottleneck for efficient inference, executing low-latency backpropagation (BP) training on lightweight hardware remains a formidable challenge. This roadblock stems from the weight-update phase, where outer-product calculations are typically performed ex-situ using auxiliary digital components, followed by serial weight updates that impose heavy latency penalties. Here, we report a stateful MXA-based outer-product engine that enables fully-parallel BP weight updates. By exploiting the physical synergy between the MXA circuit topology, the near-linear tunability of its conductance configuration, and the mathematical formalism of the outer product, we demonstrate that encoding presynaptic activations and backpropagated gradients into appropriate voltage waveforms allows for the simultaneous additive update of all memristor conductance according to the outer product of the two input vectors. We further validate this engine across various Model-Agnostic Meta-Learning (MAML) tasks, addressing the critical latency requirements for EAI. This work represents a transformative shift in the functional capability of MXAs for EAIs and on-device learning.

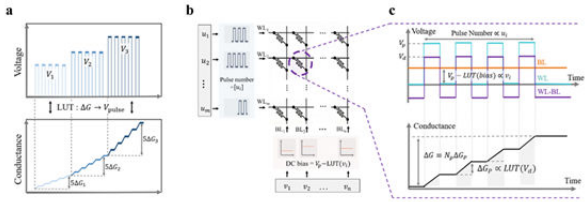


Figure 1. Architecture of the fully parallel stateful outer-product engine. a, Characteristics of a representative linear memristor. Conductance increases linearly with pulse series, and the average conductance change (ΔG) shows a positive, non-linear correlation with pulse amplitude (V_pulse), characterized by a lookup table. b, Schematic of the fully parallel incremental outer-product update scheme. c, Detailed evolution of WL/BL voltages, device voltage drop, and conductance for a typical device.

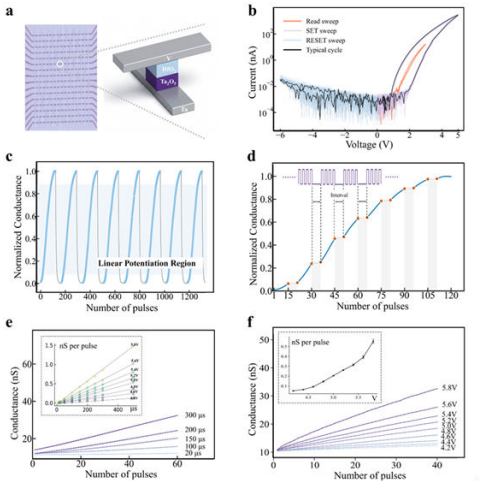


Figure 2. Structural and electrical characteristics of the highly linear memristor array. a, Schematic of the vertically stacked Ta/Ta2O5/HfO2/V/Pt device structure. b, Current–voltage (I–V) characteristics over 20 consecutive SET and RESET cycles and read sweep, demonstrating self-selective and self-rectifying behaviors. c, Conductance response to 8 consecutive programming pulse series, exhibiting continuous linear potentiation and non-linear depression. d, Evaluation of state retention and non-volatility during programming. The linear potentiation process is divided into eight segments separated by 10-second intervals to verify conductance stability. e, Conductance change per pulse as a function of the programming pulse amplitude. f, Quasi-linear dependence of the conductance change per pulse on the applied pulse width.

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A Fully Integrated Low-Power DNN Processor for In-Memory Computing Based on Non-Filamentary Nb_2O_5/CeO_2 Memristors

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Although memristors have been widely researched for energy-efficient in-memory or neuromorphic computing, several critical hurdles still limit their practical application. While filamentary memristors exhibit degraded uniformity from random formation paths and substantial power consumption near the low-resistance state (LRS), interfacial-type memristors are hindered by inadequate retention resulting from volatile ion back-diffusion. In addition, even though numerous studies have been reported at the single-device level, few have demonstrated fully integrated systems employing novel materials for the switching layer.

In this study, the interfacial resistive switching (RS) characteristics of cerium oxide (CeO_2)-niobium oxide (Nb_2O_5) bilayer memristors have been demonstrated. The Nb_2O_5/CeO_2 memristor exhibits analog RS with a large dynamic range (>10^2) and low current levels (1–500 nA) without filament formation. This is attributed to the fact that CeO_2 and Nb_2O_5 are highly suitable materials for valence change memory (VCM) owing to their tunable valence states (Ce^{3+}/Ce^{4+} and $Nb^{5+}/Nb^{4+}/Nb^{2+}$) and high oxygen ion storage and release capacity. [1,2] Furthermore, the memristor exhibits improved retention because the Nb_2O_5 layer suppresses oxygen-ion back-diffusion by functioning as an ion-holding layer, while the CeO_2 layer acts as the RS layer. [3] The memristor array enabled linear analog weight updates on the selected cell with negligible array sneak currents and disturbance under the half-bias condition, even without an additional selector. Moreover, owing to the self-selecting characteristics of the non-filamentary memristor, vector-matrix multiplication (VMM) operations could be performed with low power consumption (4–6 nW) even when all cells in the column were in the LRS.

The Nb_2O_5/CeO_2 memristors were also integrated on back-end-of-line (BEOL) complementary metal-oxide-semiconductor (CMOS) foundry wafers. The synapse array was fabricated directly on-chip over the CMOS logic, comprising DAC/ADC circuits and row/column drivers. The entire fabrication process, including the memristors, was fully CMOS-compatible. The CeO_2 RS layer was deposited via atomic layer deposition (ALD) with a precisely controlled thickness of 5–10 nm, enabling device update operations at sub 2 V. The energy consumption per device during inference was estimated to be approximately 1 fJ, demonstrating the excellent power efficiency of the fabricated DNN processor for data-centric applications.

In conclusion, this research highlights the implementation of low-power in-memory computing via non-filamentary memristors and the realization of a fully integrated system based on novel materials (Nb_2O_5/CeO_2). These results indicate that CMOS-integrated memristor systems can provide an effective hardware platform for low-power, energy-efficient in-memory computing.

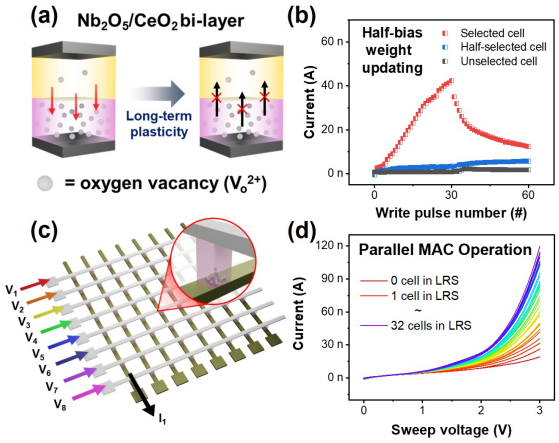


Figure 1. a) Schematic illustration of conductance change and (b) analog weight update modulation of the memristor. (c) Schematic illustration and (d) VMM measurement in the array.

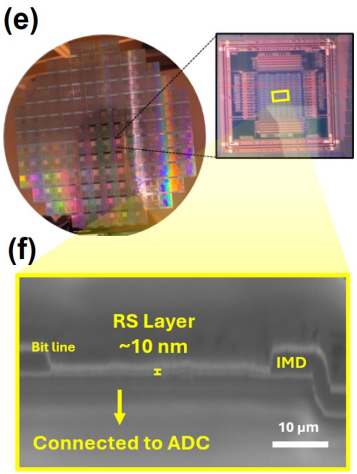


Figure 2. (e) Image of the CMOS foundry wafer (f) Cross-sectional SEM micrograph of a fully Integrated chip.

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Monolithic 3D integrated memristor array for low-interfered and high-density in-memory computing

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In-memory computing has emerged as a promising approach for energy-efficient and massively parallel data processing by reducing data transfer between memory and processing units in conventional von Neumann architectures.[1] The monolithic three-dimensional (M3D) integration of memristor arrays with silicon transistors facilitates energy-efficient parallel data processing and attains high-density arrays, representing a breakthrough approach for in-memory computing systems. In this work, we fabricated 1-kbit M3D integration of TiOx memristor (1M) and the transmission gate-inverter circuit comprising of four MOSFETs as a transistor-selector (1TS), confirming both operational voltage range and current levels between 1M and 1TS are well aligned. The transmission gate-based selector, consisting of four MOSFETs, was designed to provide robust binary inputs to selected memristor cells while effectively suppressing voltage drops and sneak-current paths. The selector exhibited a high ON/OFF ratio of 7.18 × 107, enabling reliable array operation. The fabricated 1M and 1TS-1M arrays demonstrated stable long-term potentiation and depression characteristics over 3,000 programming pulses, with tunable learning rates depending on the programming voltage schemes. Based on the measured device characteristics, the proposed 1TS-1M architecture shows potential scalability up to a 1.14 Tbit crossbar array without significant cell interference. Furthermore, this 1TS-1M array system achieved up to 79.47% and 84.89% recognition accuracies for the CIFAR-10 and UTK face images dataset, respectively, even in the limited convolution and pooling layers in the convolution neural network (CNN).

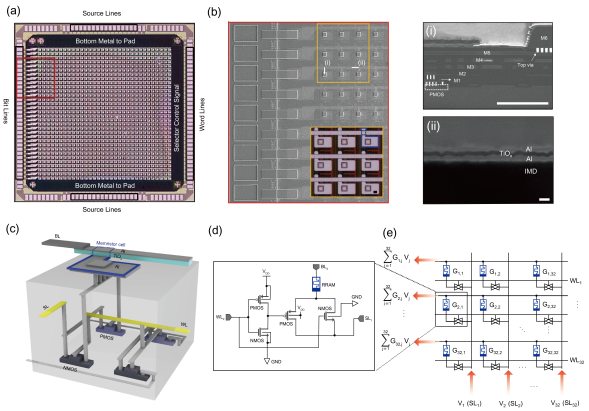


Figure 1. Fabrication of monolithically CMOS-integrated 1-kbit 1TS-1M array. (a) Optical microscopic images of the full chip containing a 1-kbit 1TS-1M array where the memristor cells are integrated atop of transistor-based selectors. (b) Scanning electron microscope (SEM) image of the region indicated by the red box of (a). The inset image shows corresponding optical microscope image of the 3 × 3 1TS-1M array denoted in the yellow box. (i) presents a cross-sectional SEM image showing the layer-stacked, monolithic integration of the PMOS and memristor in the 1TS-1M configuration. Note that other MOSFET devices are absent in the range of SEM image. (ii) shows a cross-sectional SEM image of the Al/TiOx/Al memristor integrated on the sideline of M6 surrounded by IMD layer. (c) Schematic of the 1TS-1M cell showing the connection lines (SL, BL, and WL) and each device (TiOx memristor and four MOSFETs). (d) Electrical circuit schematic of the 1TS-1M cell (e) Schematic of VMM operation in the 1TS-1M cell. Input voltages (Vn) are applied from SLn, output currents are determined from the summation of Vn and Gi,j of each node, and each 1TS can be switched by the gate voltages in the WLn lines.

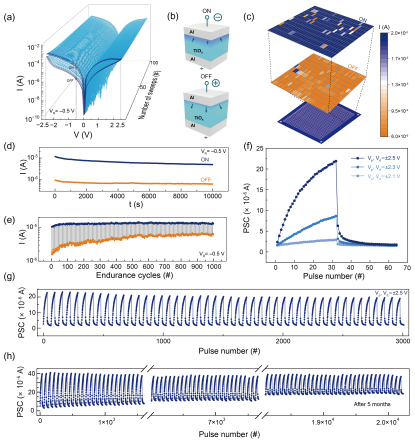


Figure 2. Electrical and synaptic characteristics of 1-kbit TiOx memristor array. (a) Robust I-V bipolar switching properties across 100 repetitive sweeping cycles. (b) Potential switching mechanism of ON and OFF states for the TiOx memristor. (c) Statistical heatmap of the ON and OFF states for 320 cells randomly selected on 1-kbit TiOx memristor array. The orange (dark blue) color in the ON (OFF) state indicates a relatively small (high) current that is comparable to the OFF (ON) state, indicating a small ON/OFF ratio. (d) Retention characteristics of the ON and OFF states over 10000 s at VR= -0.5 V. (e) Endurance cycling test over 103 cycles at VR= -0.5 V. (f) Gradual LTP and LTD characteristics of the PSC for the TiOx memristor depending on different VP(D) pulses ranged from ± 2.1 to ± 2.5 V. (g) Repetitive transitions between LTP and LTD characteristics of the PSC over 3000 pulses. VP(D) pulses are set to ± 2.5 V. (h) Repetitive transitions between LTP and LTD characteristics of the PSC over 20,000 pulses for the selected device cell that had been fabricated 5 months prior.

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Analog Resistive Switching Assessment of CMOS-Compatible Engineered HfO_2-Based RRAM Devices

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Resistive Random-Access Memory (RRAM) has attracted significant attention from the scientific community for its potential as embedded non-volatile memory owing to its CMOS-compatibility, high density, fast switching, and low power consumption [1]. More recently, RRAM technology has emerged as a promising candidate for the implementation of neuromorphic hardware, where its analog conductance modulation can emulate the gradual potentiation and depression of biological synapses, enabling highly energy-efficient computing architectures [2]. However, realizing reliable and reproducible analog switching remains a major challenge, as filamentary RRAM devices typically exhibit abrupt and stochastic conductance changes. One promising strategy to address this limitation is the optimization of the metal-insulator-metal (MIM) stack, enabling improved control over conductive filament formation and rupture and, consequently, more gradual resistive switching [3].

Motivated by this approach, this work presents a comparative experimental study of four CMOS-compatible RRAM MIM stacks fabricated on a 200 mm wafer. The various stacks differ based on the considered insulating layers, which include: a single-layer HfO_2 with 3% Al doping commonly employed for multi-level discrete-states operations [4], two $TiO_2/HfO_2/Al_2O_3$ trilayer stacks with different HfO_2 thicknesses, and a TiO_2/HfO_2 bilayer stack based on the conventional Al-doped HfO_2 dielectric. All tested RRAM devices feature a MIM area of 600 nm × 600 nm. To evaluate both cycle-to-cycle and device-to-device variability, 20 devices per material stack were characterized over 20 voltage-ramp switching cycles, resulting in 400 I-V characteristics. The various cycles, as well as the resulting median curve for the material stack, can be seen in Fig. 1. While the reference single-layer HfO_2 device exhibits abrupt evolution when transitioning from High Resistive State to a Lower Resistive State (i.e., SET operation), all three alternative engineered stacks demonstrate significantly more gradual switching behavior, highlighting their potential for analog neuromorphic applications.

To further assess their analog switching characteristic under common potentiation-depression pulsed stimuli [5], each of the three alternative insulating layers were programmed via Constant Amplitude Pulse and Verify Algorithm (CAPVA) [6]. As the voltage-ramp characteristic does not show the possibility to operate the device in a fully analog fashion, the conventional single-layer HfO_2 is discarded from this measurement campaign. Since each of the three alternative MIM stack may require different optimization in the programming condition, a systematical analysis was conducted studying different combinations of pulse width and pulse amplitude. Representative potentiation-depression characteristics obtained under one of the optimized pulse conditions for each material stack are shown in Fig. 2. These pulse conditions are selected by fitting the resulting evolution of the MIM stack conductance and evaluating its gradualness, memory window, and cyclability. The achieved characteristics show gradual evolution of the device state controllable by the number of programming pulses applied. These results further confirm the suitability of the proposed device stacks for analog resistive switching for analog in-memory computing and neuromorphic hardware implementations.

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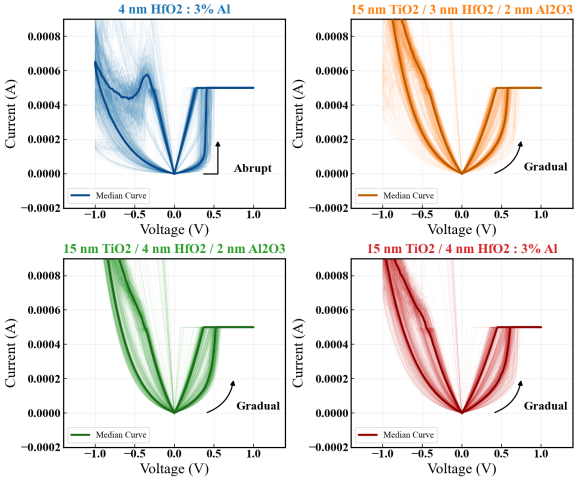


Figure 1. Aggregated DC current-voltage characteristics from 20 devices and 20 voltage-ramp switching cycles (400 cycles) for each of the four CMOS-compatible RRAM MIM stacks.

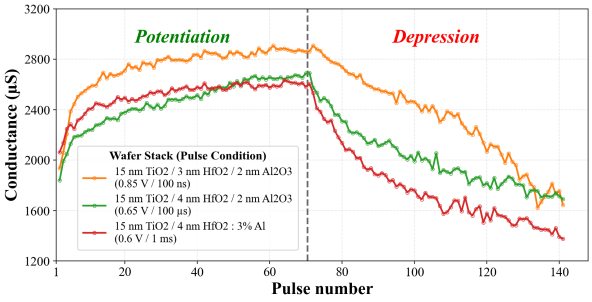


Figure 2. Potentiation and depression characteristics of the engineered RRAM MIM stacks obtained using CAPVA under representative pulse conditions.

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Talks

Electrochemical Metallization

Engineering of the volatile dynamics of Ag-based electrochemical memristors

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Artificial intelligence (AI) has dramatically increased its performance in recent years, accompanied by a parallel growth in environmental impact and energy footprint. In addition, the trend of moving AI computation from datacentres to localized edge devices has gained importance. Therefore, it is urgent on one side and strategic on the other to identify novel sustainable computing paradigms. Taking inspiration from the brain's operation is one promising approach, for which existing computing technologies lack some fundamental functionalities. The temporal dynamics typical of neurons, synapses, and dendrites, which span a wide timescale range [1], represent a crucial computing primitive of the brain that enables real-time processing with ultimate efficiency, and is difficult to implement with conventional electronic elements such as capacitors.

Volatile diffusive memristors, based on the migration and nucleation of metal cations, can emulate basic brain-inspired cognitive functions that encode information in the time domain, such as short- to long-term memory transition, spike-timing-dependent plasticity, paired-pulse facilitation and inhibition, among others. These devices display voltage-driven switching from high to low resistance states followed by self-relaxation. This behaviour arises from the complex dynamical interplay of cation formation, migration [2], and evolution of formed nuclei [3]. It can be achieved over multiple timescales, from nanoseconds to possibly minutes, through programming protocols and material design, for which clear guidelines are not yet well established.

In our lab, we investigate volatile diffusive memristors with Ag/SiOx/Pt bare structure through a two-fold approach: (i) identification of programming strategies to exploit various temporal dynamics [4,5] and (ii) material optimization towards slower temporal dynamics [6].

Through different programming strategies, we identify several switching features, like stepwise current increase during switching (Fig. 1 on the left side of the axis break) and decrease during relaxation (Fig. 1 on the right side of the axis break), integrative function both in high resistance and low resistance states. Indeed, in addition to the conventional post-programming relaxation dynamics, we evidence a hidden dynamic, which is internal to the device, and which fulfils an additional integration function. This effect is not associated with a measurable current and therefore offers an energy advantage compared to the commonly studied low resistance relaxation dynamics.

Through engineering of an Al2O3 interlayer inserted at the Ag/SiOx interface, we demonstrate the possibility to extend the tempoeral scale of device dynamics by orders of magnitude, as already visible from current-voltage characteristics in Fig. 2. Ag/1-2.5 nm Al2O3/SiOx/Pt, compared to bare Ag/SiOx/Pt devices, show longer relaxation dynamics. Furthermore, only in devices with Al2O3 interlayer an appreciable recovery time is needed to obtain a dynamic response that is equivalent to that shown by fresh devices. Such reovery time is an additional temporal dynamics useful for emulation of brain inspired computing primitives.

The results highlight relevant physical aspects underlying Ag-based volatileve diffusive memristors and contribute to identication of programming strategies and material engineering approach for achieving multi-timescale device dynamics.

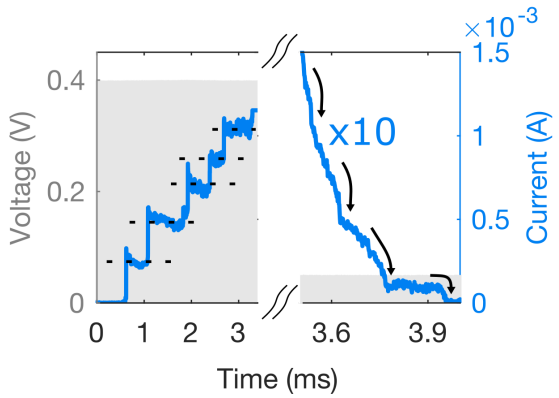


Figure 1. Stepwise current increase during switching (left side) and decrease during relaxation (right side): applied voltage (grey, left y-axis) and current (blue, right y-axis) as a function of time.

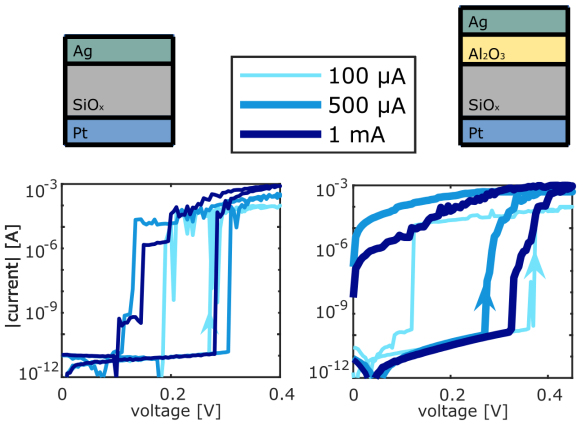


Figure 2. Current voltage characteristics of Ag/SiOx/Pt and Ag/2.5nm Al2O3/SiOx/Pt devices at different values of the current compliance. Device with Al2O3 interlayer show nonvolatile sweeps at higher compliance.

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Overcoming Filament Stochasticity: RESET-Based Programming in Electrochemical Metallization Memristors

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Filamentary memristive devices for neuromorphic computing face a significant challenge: stochastic filament growth leads to high cycle-to-cycle variability[1], hindering the development of reliable multilevel analog computation and reproducible synaptic weight programming. Here, we demonstrate a strategy that employs partial RESET processes to program reproducible multilevel quantized conductance states(QCS) with minimal variability in Ag/SiO_2/Pt electrochemical metallization cells. By leveraging gradual atomic dissolution through electrochemical polishing[2] (ECP), this RESET-based approach fundamentally suppresses the stochasticity inherent in filament growth, and achieves exceptional state retention exceeding 62,000 seconds at room temperature in ambient air. With deeper investigation, we identify three distinct RESET modes: (1) initial RESET, in which quantized conductance evolution produces stable QCS with state retention exceeding 4600 s; (2) negative SET during RESET, in which spontaneous quantum point contact reformation during voltage relaxation yields quasi-equilibrium states with 5000 s retention; and (3) partial RESET, which exhibits pathway-independent convergence to reproducible quantized conductance states, achieving a record retention of 62,000 s. This RESET-based mechanism fundamentally differs from conventional approaches, thereby overcoming the high variability inherent in filament growth. This mechanism enables reproducible multilevel control, positioning RESET-based programming as a practical route toward reliable analog memristors for neuromorphic hardware, in-memory computing, and quantum resistance standards.

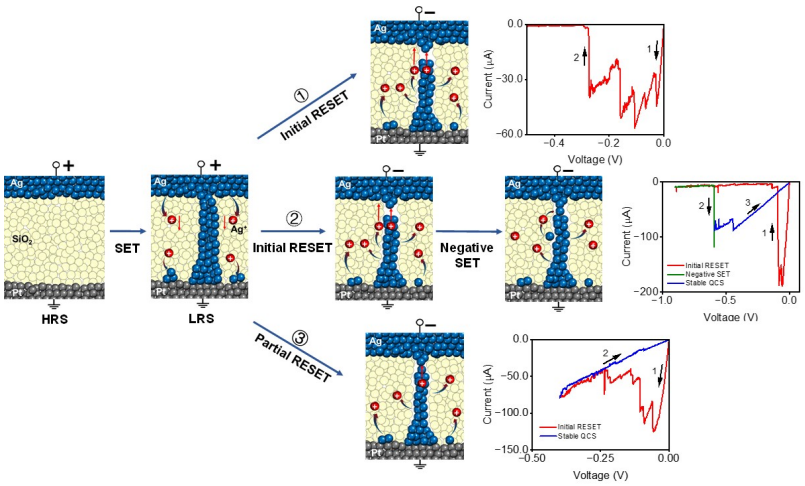


Figure 1. Schematic models demonstrate three different RESET behaviors.

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Localizing Switching Sites: Low-Variability ECM Memristors via On-Chip Ag NP Synthesis

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Variability in performance is a longstanding challenge for electrochemical metallization cell (ECM) memristors[1]. In conventional devices, crossbar architectures are employed with blanket, unpatterned active electrodes (AE), promoting parasitic overdeposition of active metal (e.g. Cu, Ag) upon operation and thus variability. In previous studies, restricting the active metal at the AE-dielectric interface via structures like nanodots[2] or nanoporous Pt[3], proved highly efficient in reducing set voltage variability, cycle-to-cycle and device-to-device.

Here we report on a new lithography-free, on-chip Ag nanoparticle (NP) synhtesis method for ECM memristors with <10% relative standard deviation spread in set voltage. A carbon-free, wet-chemical synthesis method is used to nucleate Ag NPs stochastically on the interface between dielectric (SiO2) and top electrode passivation metal (Pt). A SEM image of a device and a cross-section sketch are displayed in Fig. 1. The NP formation takes place on-chip and requires no extra surface preparation. The R-V hysteresis of a representative device is shown in Fig. 2, indicating excellent switching stability while retaining low set voltages and high Roff/Ron ratios. We quantify cycle-to-cycle and device-to-device variability, endurance and fabrication yield. The device physics is explored by presenting evidence of switching site localization at the Ag NP and systematic variations of NP size and density.

This proof-of-concept work demonstrates a new fabrication route for low-variability ECM memristors. This work establishes on-chip Ag NP synthesis as a simple, lithography-free route to localize filament formation and suppress variability in ECM memristors.

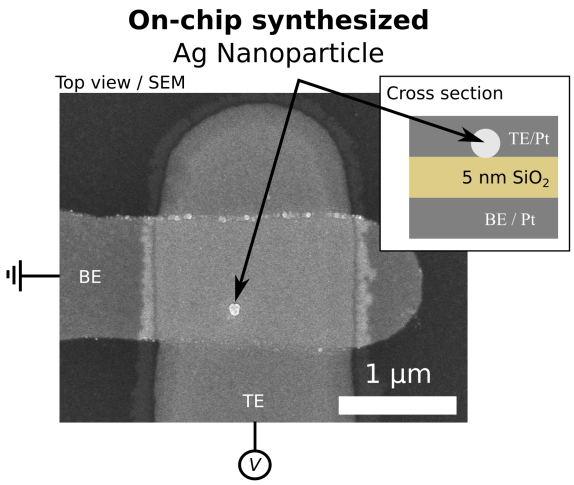


Figure 1. SEM of the final crossbar memristor structure and sketch of the device cross-section (inset). The on-chip synthesized Ag nanoparticle is marked with arrows. The top and bottom electrodes are denoted with TE and BE respectively.

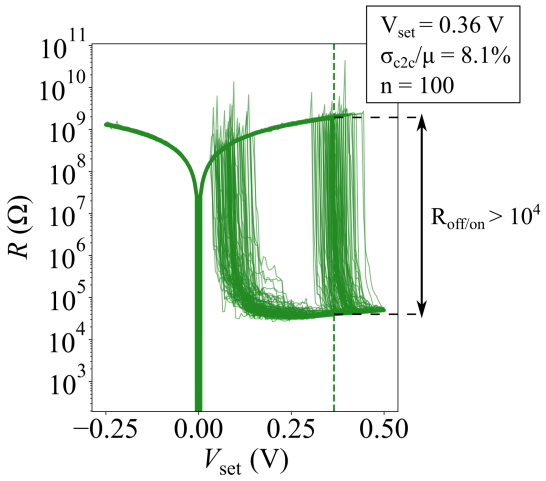


Figure 2. Exemplary R-V hysteresis of a memristor enabled by on-chip synthesized nanoparticles. Set voltage, variability and cycle number are denoted in the inset. The Roff/Ron ratio is given on the right.

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Direct operando STEM observation of coupled Cu filament dynamics in hafnia-based memristors

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The implementation of filamentary memristors for next generation neuromorphic computing is heavily hindered by stochastic switching and reliability issues, stemming from a limited understanding of nanoscale conducting filament dynamics. Here, we report an operando scanning transmission electron microscopy (STEM) investigation combined with multi dimensional chemical and structural analyses, including electron energy loss spectroscopy (EELS) and 4D-STEM of Cu/HfO2/Pt device. We reveal that a native interfacial oxidation gradient dictates the stochastic nucleation of discrete metallic Cu nanodots. These localized nanodots induce severe electric field confinement and enhancement, triggering a localized ”winner-take-all” competitive filamentary growth. Crucially, we establish a comprehensive switching model governed by intrinsic coupling between nanoscale filament dynamics and the redox front movement within the electrode. While the set process involves concurrent filament growth and reservoir expansion, the reset process triggers a dual dissolution mechanism, effectively rupturing the filament while re-oxidizing the reservoir. Furthermore, this interfacial coupling effect offers a universal design strategy to suppress stochasticity, showcasing a strong synergy with VCM based memristors. This work underscores that the electrode actively contributes to the resistive change, offering crucial interfacial design strategies for high reliability neuromorphic applications.

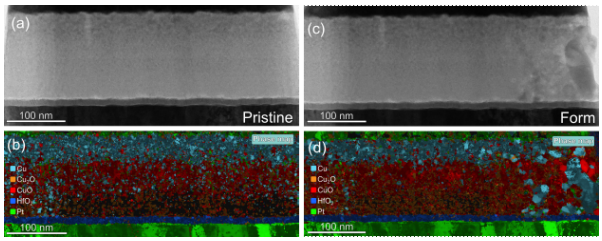


Figure 1. Operando structural and phase evolution of the memristor during the electroforming process. (a, c) Cross sectional bright field (BF) images and (b, d) corresponding ACOM phas maps of the device in its (a,b) pristine state and (c,d) after the electro forming process. The native oxidation gradient layer, comprised of stacked and phases, is clearly resolved at the upper electrode interface adjacent to the switching matrix.

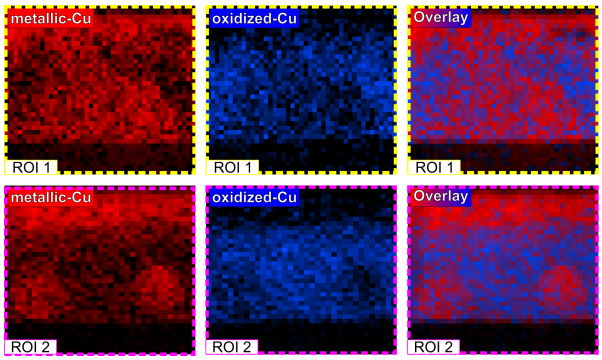


Figure 2. Spatial distribution of Cu chemical states resolved by MLLS (Multiple linear least squares) fitting: (j-1 to j-3) metallic Cu, oxidized Cu, and their composite overlay for ROI 1. (k-1 to k-3) metallic Cu, oxidized Cu, and their composite overlay for ROI 2.

Different modes of threshold switching in Ag/HfO2/Pt-based volatile electrochemical metallization memory (v-ECM) devices

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Volatile electrochemical metallization memory (v-ECM) cells show interesting properties for neuromorphic computing applications [1]. The devices exhibit threshold-type switching from a very high resistive state to an ON-state when the voltage rises above the threshold voltage. When the voltage on the device drops below the hold voltage, the v-ECM cell returns to its high resistive state. The characteristic time of this relaxation process, called relaxation time, depends on the programming conditions, namely, the voltage amplitude and the duration [2,3]. A compact model for v-ECM cells has been developed that can successfully describe the SET kinetics, which describes the SET time required for a given SET voltage of Ag/HfO2/Pt-based v-ECM cells [4]. The model includes electrocrystallization, electron-transfer reactions at the interfaces and ionic migration as rate limiting processes. Recently, a counteracting force, the electromotive force EMF, has been added in the equation system enabling the simulation of volatile switching effects, mainly the return to the high resistive state when the voltage falls below the hold voltage.

In this work, we study v-ECM devices based on Ag/HfO2/Pt crossbar structures (Fig. 1) with differences in their current-voltage behavior regarding the characteristic values of the threshold and hold voltage. We show how the threshold voltage of the v-ECM devices can be controlled and analyze the SET kinetics behavior of the different switching modes. We apply the JART v-ECM model [4] to simulate the threshold-type switching characteristics (Fig. 2) and discuss the most significant differences of state variables between the modes in this presentation. The model is implemented in Verilog-A and is used to simulate leaky-integrate-and-fire function. The simulation model can be further utilized for the design of more complex neuromorphic circuits and systems.

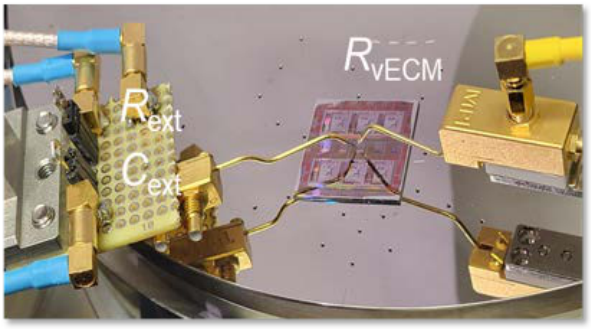


Figure 1. Breadboard setup of an integrate-and-fire circuit with the Ag/HfO2/Pt v-ECM device in the center.

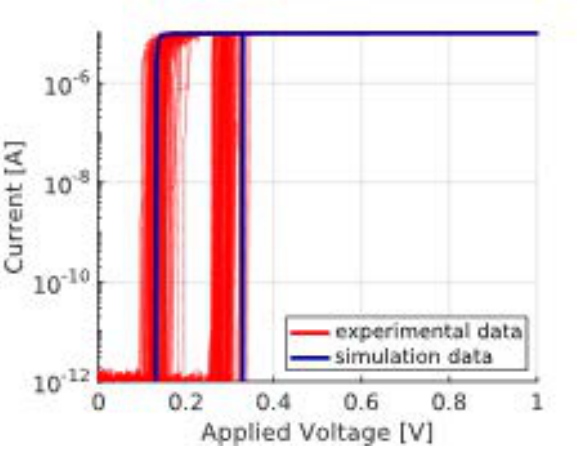


Figure 2. Measured I-V sweeps of an Ag/HfO2/Pt v-ECM cell (red) and an I-V sweep (blue) simulated by the v-ECM model (from [4]).

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Synaptic Dynamics in Soft Metal–Polymer Formulations for Neuromorphic Computing

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The search for materials capable of replicating both the structural and functional characteristics of biological synapses establishes a natural pathway towards memristive hardware systems approaching biological performance metrics. Iontronic-based systems have attracted significant interest owing to their biorealistic electroionic nature, with recent reports demonstrating near-biological voltages and energy consumption, as well as synaptic plasticity [1,2]. Of the various material platforms, soft materials have emerged as promising candidates due to their similarity with biological synaptic environments; among these, poly(vinyl alcohol) (PVA) stands out as an attractive polymeric host due to its green, biocompatible, and cost-effective nature [3]. In aqueous solution, PVA may form a gel-like matrix with high mechanical compliance, easy processability, and environmental compatibility. Additionally, the incorporation of ionically active species, such as metal ions (Ag^+, Cu^{2+}), extensively reported for their high ionic mobility and well-established electrochemical behaviour, has demonstrated strong potential for emulating the role of neurotransmitters [2,4].

This work reports the fabrication and comprehensive investigation of soft PVA-based memristive devices doped with $AgNO_3$ or $CuSO_4$ [5]. Six formulations with varying metal salt concentrations (0.05–1 mol/L) were prepared using PVA as the polymer host and deionised water as the solvent medium. Devices were fabricated in a counter-electrode (grounded Ag or Cu plate) / electrolyte layer (PVA:$AgNO_3$ or PVA:$CuSO_4$) / working electrode (Pt wire) configuration, intentionally designed to emulate a presynaptic / synaptic cleft / postsynaptic neuronal arrangement.

Electrical characterisation demonstrated that both systems exhibit bipolar resistive switching (sub-100 mV for PVA:$AgNO_3$ and sub-500 mV for PVA:$CuSO_4$) with highly reproducible endurance behaviour (>10^4 cycles) and state retention capability (>3600 s). Both demonstrated long-term potentiation and depression (LTP/LTD), paired-pulse facilitation and depression (PPF/PPD), and spike-timing-dependent plasticity (STDP), collectively spanning key forms of Hebbian and temporal learning rules associated with memory consolidation and adaptive behaviour in biological neural circuits.

The switching behaviour is consistent with a purely interfacial electrochemical mechanism driven by metal-ion redistribution and localised redox reactions at the electrode–electrolyte interface, offering the advantages of interface-confined switching control and predictable reaction kinetics [2,5].

To validate functionality, experimental conductance data were directly embedded into a multilayer perceptron (MLP) and trained on the MNIST dataset, showing pattern-recognition accuracies of 88.5% (PVA:$AgNO_3$) and 89.2% (PVA:$CuSO_4$) after 50 epochs.

These findings establish PVA-based electrolytes as promising soft iontronic memristive platforms capable of combining biorealistic switching dynamics and synaptic functionality, with potential for scalable neuromorphic computing applicability.

This work was financially supported by FCT through the projects LA/P/0095/2020, UID/04968/2025, UIDP/04968/2025, UIDB/ 04968/2025, PTDC/NAN-MAT/4093/2021, and 2022.15710.UTA. The project leading to these results also received funding from “la Caixa” Foundation under the project code LCF/PR/HR22/00189.

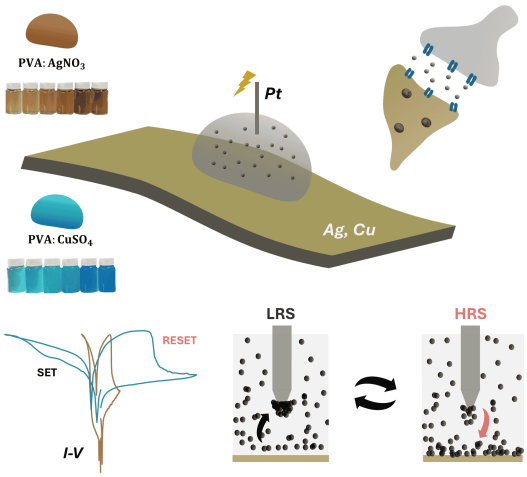


Figure 1. Schematic representation of the soft PVA-based memristive system and its biological synapse analogy, illustrating the concentration gradient metal salt-doped polymer formulations, device architecture, representative I–V characteristic, and the interfacial electrochemical switching mechanism.

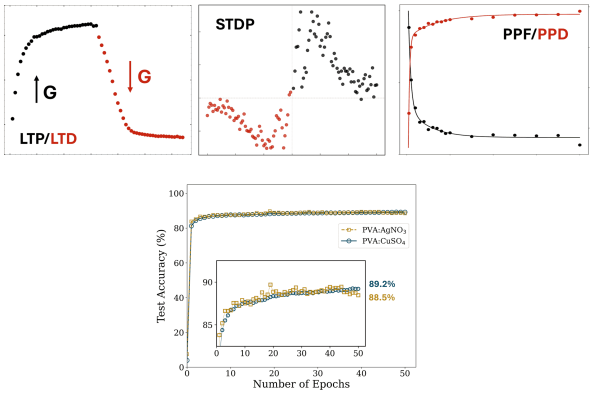


Figure 2. Representative synaptic-like plasticity responses and classification accuracy resulting from experimentally measured conductance modulation.

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Talks

Opticalelectronic Memristors

Dye-sensitized Optoelectronic Synapses for Physical Reservoir Computing-based Motion Vision Systems

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With the rapid advancement of edge artificial intelligence (AI) and the Internet of Things (IoT), there is an urgent demand for energy-efficient hardware capable of processing complex temporal and spatial data in real time. Traditional Von Neumann architectures suffer from high power consumption and latency due to continuous data transfer between memory and processing units. To overcome this bottleneck, physical reservoir computing (PRC) has emerged as a promising computing paradigm that utilizes the intrinsic physical dynamics of materials to process time-series signals directly at the sensor level. In particular, vision-inspired optoelectronic synapses that integrate sensing, memory, and processing functionalities are highly attractive for building low-power, intelligent in-sensor computing platforms.

In this work, we present a photovoltaic-type optoelectronic synaptic device based on dye-sensitized solar cells (DSCs) incorporating TiO2 nanoparticles (NPs), designed specifically for dynamic motion vision systems and PRC applications. Unlike conventional photoconductive synaptic devices that rely on slow surface oxygen adsorption/desorption kinetics, our DSC-based synapses exploit photogenerated carrier dynamics and electrochemical reactions at the porous TiO2/electrolyte interface. This operating mechanism endows the device with rich, biologically relevant temporal response dynamics on the order of seconds, which is essential for short-term memory and reservoir functionality. The developed DSC-based optoelectronic synapse exhibits excellent functional adaptability to varying optical environments. Key synaptic behavior, such as tunable response times and reversible output polarity, can be dynamically modulated by adjusting the light intensity and illumination wavelength. This spectral and temporal adaptability allows the device to function simultaneously as a self-powered photodetector and an adaptive processing unit.

To demonstrate its capability in complex real-time computational tasks, the DSC synaptic device was employed as a physical reservoir layer to classify human motion patterns. Various human activities (e.g., bending, jumping, running, and waving) were encoded into optical pulse sequences and fed into the device. Owing to the intrinsic nonlinear fading memory and wavelength selectivity of the DSC system, the inferred outputs successfully matched the desired activity categories with high classification accuracy.

In conclusion, our approach highlights the potential of leveraging photoelectrochemical dynamics in dye-sensitized nanostructures to design sustainable, intelligent edge AI hardware. We will detail the device architecture, operating mechanisms, and performance evaluations within the context of motion recognition, and discuss future prospects for multi-wavelength adaptive PRC vision systems.

Acknowledgment: This work was partly supported by JST (Grant Numbers JPMJFS2144 and JPMJSP2151), JSPS KAKENHI (Grant Numbers JP25KJ2114 and JP26K01350), the Murata Science and Education Foundation, and the TUS Program for Nurturing Top-Level Researchers.

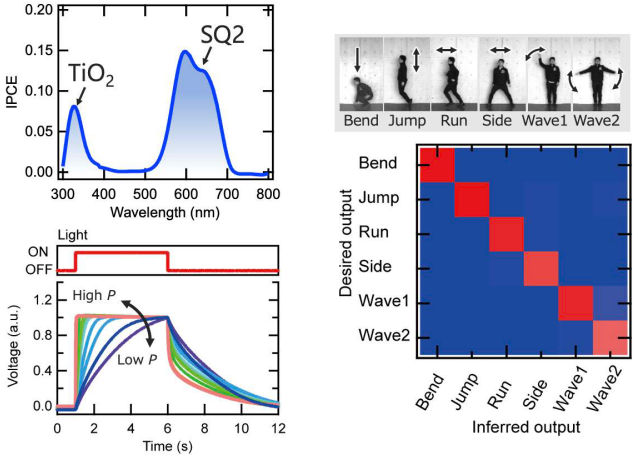


Figure 1. Photovoltaic-type optoelectronic synaptic devices using dye-sensitized solar cells and their adaptive response characteristics and human motion pattern classification performance.

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Parallel Optoelectronic programming of IGZO RRAM devices with a micro-LED array

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Light-responsive memristive hardware offer a promising pathway toward energy-efficient, high-bandwidth neuromorphic systems by enabling direct interaction between optical stimuli and electronic memory states [1]. In this work, we present optically sensitive, form-free indium–gallium–zinc oxide (IGZO) resistive random-access memory (RRAM) devices and demonstrate their suitability for parallel optical programming and spatial information encoding. These devices exhibit resistive programming and short-term memory behaviour without requiring an electro-forming step, making them attractive for scalable neuromorphic hardware implementations. The active layer is comprised of a dual-stack of 12.5 nm oxygen-rich IGZO and 12.5 nm IGZO. Optical programming is enabled through a transparent indium-tin-oxide (ITO) top contact and the broad absorption spectrum of IGZO. Oxygen-deficient defects in amorphous IGZO introduce localized electronic states that realise programmable resistive behaviour [2]. The optical probing setup (see Fig. 1a) brings the capability of a bespoke micro-LED array with flip-chip integrated CMOS driver [3] for spatial coupling of individual 450 nm blue sources onto a chip of optically sensitive RRAM devices, allowing programmable optical stimulation of multiple devices. The system combines collimation and focusing optics with real-time imaging to ensure alignment, while electrical readout uses low-disturbance voltage pulses.

Here, we characterize the electrical, optical and optoelectronic response of individual IGZO RRAM devices before demonstrating parallel spatial optical programming through multiple micro-LED to IGZO RRAM channels. For electrical characterization, resistance is programmed using a ±2 V pulse ramp, as shown in the resistance-voltage plot in Fig. 1b. Under optical excitation, the IGZO devices exhibit gradual resistance reduction, corresponding to an increased conductance (see Fig. 1c). We demonstrate that controlled optical pulse trains of varying frequency, pulse width and optical power each enable incremental state modulation, demonstrating analog-like programmability. We also demonstrate that resistive states can be reset electrically using short negative voltage pulses, enabling repeatable optoelectronic control (see Fig. 1c). These results highlight the coexistence of optical potentiation and electrical depression mechanisms with an inherent synaptic plasticity or fading memory. Utilizing full system capability, we also demonstrate parallel spatial programming with the micro-LED array addressing multiple RRAM devices simultaneously. As shown in Fig. 2, a one-to-one mapping between four micro-LEDs and four IGZO devices is used to encode 4-bit binary patterns. For each “1” bit, a micro-LED delivers an optical pulse train, reducing device resistance, whereas each “0” bit receive no illumination, preserving a high resistance state. Sequential programming of all 16 patterns, with intermediate electrical resets, confirms reliable spatial encoding with clear separation between resistive states.

In summary, we demonstrate programmable optoelectronic form-free IGZO memristive devices whose conductance increases in response to 450 nm light. Deploying a bespoke micro-LED array platform, we were able to program multiple independent devices simultaneously, allowing for the parallel writing of spatial patterns across the chip of memristive devices. During the conference we will elaborate on these results, presenting in more detail device fabrication, characteristics and fading memory applications. Overall, this approach highlights the benefits of merging photonics and electronics for the development of fast, parallel, low-power neuromorphic and in-memory computing systems.

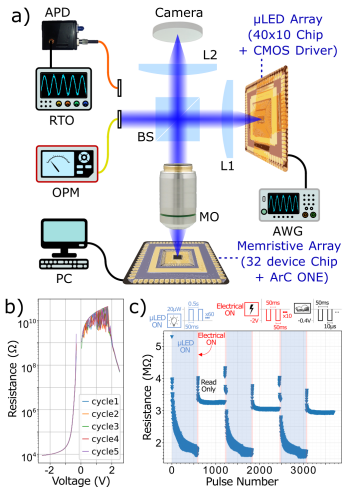


Figure 1. (a) Optical probing setup for coupling 450 nm light from a micro-LED array into optically sensitive IGZO memristive devices, enabling spatially controlled optical programming and electrical readout. (b) Electrical characterisation of resistive programming using a ±2 V voltage pulse ramp. (c) Optoelectronic programming of device resistance states under optical stimulation, demonstrating gradual resistance reduction and electrical reset recovery.

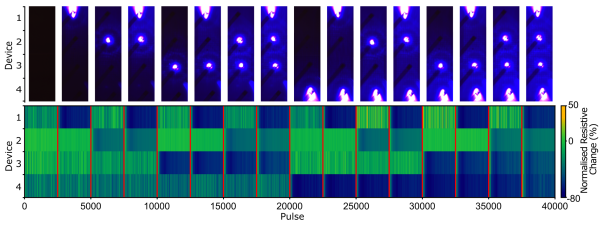


Figure 2. Spatial encoding of 4-bit patterns using a micro-LED array and an IGZO memristive array. (top) Camera images of the parallel pumping capability, four devices in total. (bottom) Colormap of electrical readout following optical programming. RRAM devices receiving optical input produce a negative resistance change (blue).

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GeSbTe Optical Memristor Devices for Neuromorphic Computer Vision

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Optical memristors are emerging devices that combine memristor behaviour with optical functionality, leveraging the benefits of light to modulate memristive states or allowing electrically controlled modulation of optical signals in photonic architectures [1]. By exploiting the unique properties of light, optical memristors introduce an additional degree of freedom for neuromorphic computing, offering pathways toward ultrafast, energy-efficient, and high-bandwidth information processing. These capabilities are particularly attractive for next-generation neuromorphic photonics and computer vision systems.

Despite their promise, significant challenges remain before optical memristors can be deployed in practical computing platforms, including improving optical responsivity, wavelength selectivity, and device scalability. To address these limitations, our group is investigating a diverse range of light-responsive materials and device architectures, including quantum dots, phase-change materials, functionalized metal-oxide thin films, and hybrid organic–inorganic nanostructured systems [2][3].

Among these candidates, the phase-change material GeSbTe (GST) has emerged as a particularly promising platform. We have developed and evaluated several GST-based optical memristor architectures, including nanoparticle thin films, continuous thin films, and co-deposited composite structures. These devices exhibit a rich range of optoelectronic switching behaviours arising from the interplay of photoexcited charge trapping, enhanced photoconductivity, and optically induced thermal phase transitions.

Fig. 1 illustrates a representative GST nanoparticle device in which UV illumination dynamically modulates the memristive hysteresis, effectively opening and closing the switching window. The response is rapid (<1 μs), highly controllable, and reproducible over repeated operating cycles. Fig. 2 further demonstrates reversible optical tuning of the memristance state under pulsed UV illumination, enabling repeatable multilevel modulation of device resistance under different optical powers.

This presentation will compare the performance and switching characteristics of the various GST-based systems and place these results within the broader context of our ongoing efforts to develop high-performance optical memristors across multiple material platforms. The findings highlight the potential of GST optical memristors as enabling components for neuromorphic computer vision and photonic computing technologies.

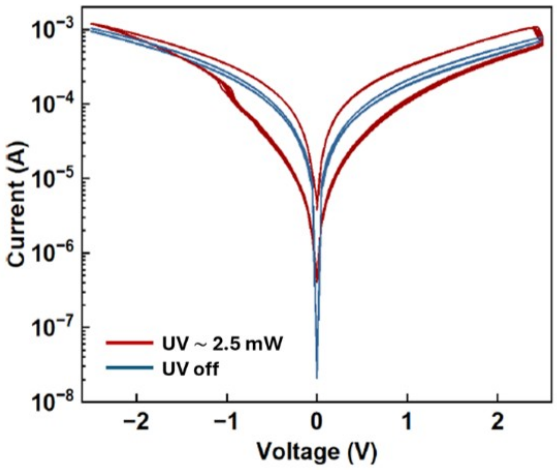


Figure 1. Current–voltage (I–V) characteristics of a GST nanoparticle memristor measured under dark (blue curve) and UV-illuminated conditions (red curve), demonstrating reversible optical control of the memristive hysteresis.

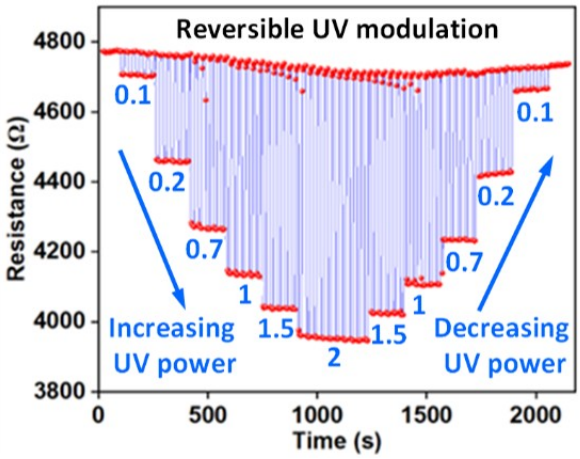


Figure 2. Resistance evolution of a GST nanoparticle memristor under pulsed UV illumination with varying optical power, showing controllable, repeatable, and multilevel modulation of the memristance state.

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Reconfigurable quantum dot light emitting memristor for neuromorphic computing

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Bio-inspired memristors have attracted growing attention as energy-efficient systems for in-memory neuromorphic computing, owing to their ability to integrate physical signal processing and information storage while emulating both short-term dynamic plasticity and long-term memory retention. However, most neuromorphic devices rely primarily on electrical conductance modulation, while optical responses are often treated as auxiliary readouts rather than computational variables. Here, we propose a reconfigurable quantum dot light-emitting memristor (QLEM) that functionally separates optical and electrical signals for neuromorphic operation. Especially, quantum dots serve as an active light-emitting medium that converts electrically driven memristive dynamics into electroluminescent optical outputs, enabling the direct use of light emission as a computational signal. In this framework, electroluminescence is used as short-term reservoir signal because of its nonlinear, fast, and history-dependent transient dynamics, while conductance is used as a long-term memory signal owing to its stable electrical state modulation. By assigning these two outputs to different computational roles, the proposed QLEM successfully realized dynamic optical reservoir processing and linear conductance-based memory operation within a single memristor, in which the electrical conductance serves as a trainable weight state during the learning process. The resulting neuromorphic system successfully enabled action recognition with a high accuracy of 91.11%, achieving a performance comparable to that of software-based learning. This dual-output QLEM strategy provides a promising route toward compact neuromorphic hardware that integrates short-term temporal processing and long-term information storage in a single device.

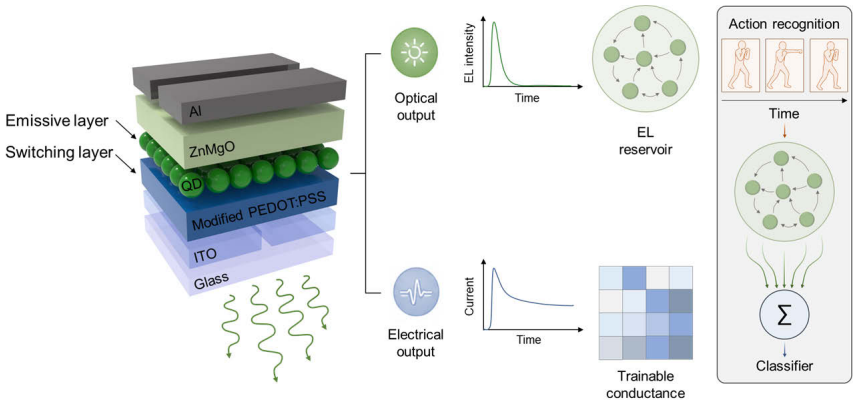


Figure 1. Overall system of QLEM-based neuromorphic computing

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Optically Tunable CuxO Based Memristor for Neuromorphic Computing

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In classical computers a significant amount of energy is consumed for the data transfer between memory and processing units due to the Von Neumann architecture. This intensified the search for alternative computing paradigms. Neuromorphic computing, inspired by the architecture of the human brain, offers a compelling path forward through in-memory computing, massive parallelism, and low-energy information processing. Central to this approach is an artificial synapse, a device that can emulate the plasticity and learning rules observed in biological neural systems.

In this work, we demonstrate an optically tunable artificial synapse based on a P-type copper oxide with an Ag/CuxO/FTO architecture. Mixed-phase CuO/Cu2O thin films were synthesized by thermal oxidation of sputtered Cu films, yielding a direct band gap of ∼1.96 eV. The device exhibits stable bipolar analog resistive switching with a large memory window and endurance exceeding 200 cycles. Electrical transport analysis indicates space-charge-limited conduction and filamentary switching governed by oxygen-vacancy migration. Under 633 nm illumination, pronounced optical tunability is observed, arising due to the photovoltaic effect mediated by the Schottky barrier and photo-generated oxygen vacancies.

The memristor successfully emulated essential synaptic functions, including long-term potentiation (LTP), long-term depression (LTD), and spike-timing-dependent plasticity (STDP), with gradual, symmetric conductance modulation. Optical stimulation further enhances synaptic behavior, enabling light-assisted LTP/LTD, light-induced short-term plasticity, and optical paired-pulse facilitation (OPPF), closely resembling retinal synaptic responses. Furthermore, Pavlovian classical conditioning is demonstrated using combined electrical and optical stimuli, revealing device-level associative learning and extinction characteristics.

To assess the neuromorphic computing potential of the device, experimentally obtained conductance values from LTP and LTD measurements were used as synaptic weights in a single-layer perceptron neural network to perform image classification on the MNIST dataset. Using off-chip training, the device-based network achieved a classification accuracy of 89.62%, which is comparable to the software-weight-based classification.

These results demonstrate that the Ag/CuxO/FTO memristor is a promising platform for energy-efficient neuromorphic vision sensors and artificial intelligence hardware, owing to its dual electrical and optical controllability and its ability to emulate biologically relevant synaptic plasticity.

Keywords: Optical memristor, Optoelectronic synapse, Optical paired-pulse facilitation, Pavlovian conditioning, Neural network.

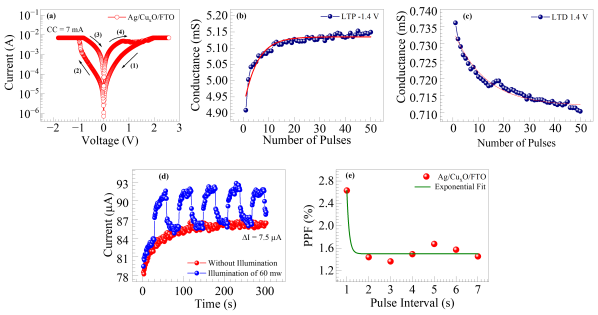


Figure 1. (a) I-V (b) LTP and (c) LTD Characteristics of the memristor (d) Response of the memristor to 633 nm 60 mW optical stimuli (e) Emulation of OPPF Characteristics

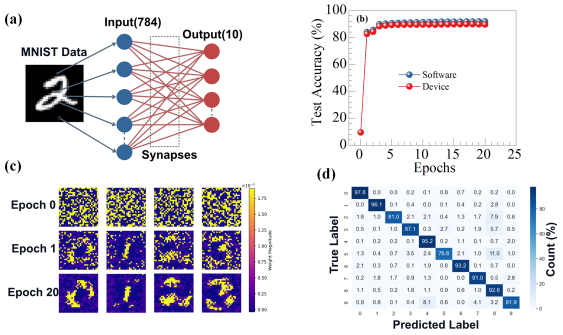


Figure 2. (a) Schematic of the perceptron neural network. (b) Test accuracy (%) as a function of the number of training epochs for the software and synaptic device-based networks. (c) synaptic weight maps of the perceptron network for the epochs 0,1 and 20. (d) Confusion matrix for the synaptic device-based perceptron network.

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Talks

VCM / Modelling

The Role of Materials and Defects on the Electroforming and Switching Mechanism of Filamentary VCM Cells

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Memristive devices based on the filamentary valence change mechanism (VCM) recently entered the market as embedded non-volatile memory. They rely on the thermally assisted motion of ionic defects within a filamentary region of an oxide thin film. Initially, the metal/oxide/metal VCM devices need to be electroformed, which leads to the formation of the oxygen-deficient filamentary region by the extraction of lattice oxygen. Thus, microscopic ionic processes determine parameters such as forming voltage, switching dynamics and filament formation. To study the influence of microscopic effects on device behavior, kinetic Monte Carlo (kMC) simulations are a viable tool.

In this work, a kMC model for electroforming and switching of filamentary VCM cells is presented that is based on creation of oxygen vacancies via redox reactions at the interfaces, oxygen vacancy transport, Joule heating and current transport calculation[1]. Using this model, the electroforming process is investigated [2]. The parameters studied are the role of the electrode materials, an initial sub-stoichiometry of the oxide, the applied voltage amplitude, and the ambient temperature. Moreover, the role of inhomogeneous oxygen defect migration barriers is investigated to explain short-term noise and long-term retention phenomena consistently [3]. In addition, it is discussed how the materials inhomogeneity (e.g., by doping) could stabilize the filament.

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Nanoscale Filament Evolution and Local Resistive Switching in Sub-Stoichiometric Yttrium Oxide Thin Films

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Scaling resistive random-access memory (RRAM) toward ultra-dense crossbar arrays for high-density storage and neuromorphic computing requires precise nanoscale control of conductive filament evolution for reliable multi-level operation. Here, we directly visualize nanoscale filament evolution in sub-stoichiometric Y2O3-x thin films using in-situ conductive atomic force microscopy (c-AFM) with independently controlled current compliance, as demonstrated in Fig. 1. The threshold voltage follows the tuned oxygen stoichiometry, while the conductive filaments governing switching can be continuously modulated through controlled external biasing, in good agreement with the macroscopic device's characteristics [1,2]. Multicycle measurements reveal that the dominant filaments persist and govern subsequent switching events. Single-point switching demonstrates nanoscale operation with a lateral influence of ∼20 nm, as shown in Fig. 2, defining the minimum practical device spacing. These results uncover the interplay between oxygen stoichiometry, filament evolution, and device scaling, establishing design and operation guidelines for next-generation ultra-dense yttrium-oxide-based memristor arrays.

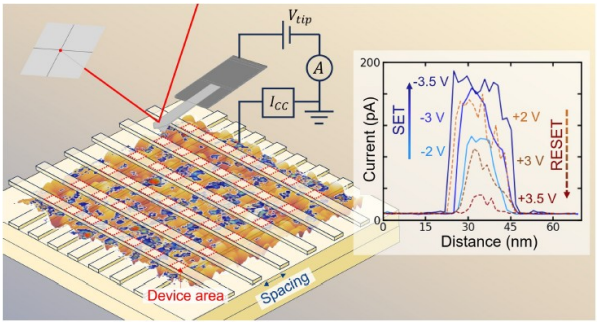


Figure 1. Illustration of c-AFM setup with current compliance and direct visualization of nanoscale filament evolution. Current profile of the filament at a single filament during SET and RESET processes. All current profiles are measured with read bias of +0.25 V.

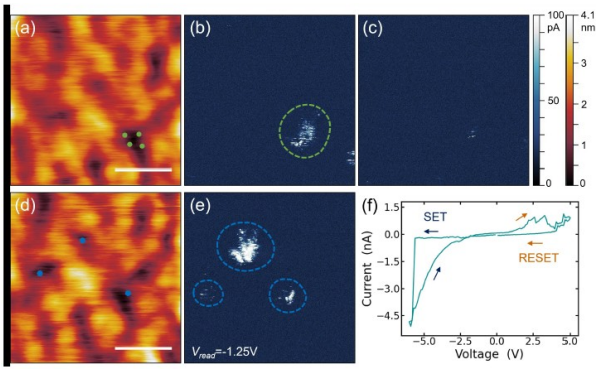


Figure 2. Single-point resistive switching and single-point I-V sweep. (a) Initial state topography. The four green dots indicate the locations for single-point switching. (b) current map of the area of (a) upon the individual SET with -6 V applied at the four green points marked in (a), and read out at tip bias -1.25 V. The green dashed circle highlights the current arising from the SET process. (c) The current map after the +3 V full-area RESET process and read at -1.25 V, showing that the set-induced current is significantly reduced. (d) Topography after SET and RESET operations, with three blue dots marking spatially separated sites for the next individual switching cycle. (e) The current map measured upon three individual single-point SET processes, with the currents induced by the SET processes highlighted by the blue dashed circles. The white scale bars are 50 nm. (f) single-point IV switching at a grain boundary.

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Forming voltage reduction of 1T1R RRAM devices by tuning Ti/Al:HfO2 thickness ratio while maintaining reliable switching performance

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RRAM devices have garnered attention as a promising solution to overcome the Von-Neumann bottleneck in data processing, owing to their capabilities for non-volatile memory storage, CMOS-compatible fabrication, and a simple device structure that facilitates easier integration into existing CMOS technologies [1]. RRAM device switching characteristics, such as forming, set/reset, endurance, and retention, are primarily influenced by the switching material and the metal electrodes composing the device. This is due to the type of oxygen exchange layer (OEL) deposited between the switching layer and the top electrode, which facilitates the switching process [2]. Although many studies have examined the effects of OEL thickness while keeping the switching layer thickness constant [3], variation in both thicknesses, while keeping the ratio constant, is needed to fully understand the influence of the OEL on the switching characteristics. A challenge also remains for 1T-1R devices regarding layer thicknesses due to the voltage stress that can be induced in the transistor at higher forming voltages.

In this work, variations in the Ti (OEL) and Al-doped HfO2 switching layer thicknesses, while keeping their ratio constant in 1T-1R devices, are investigated to understand the effects on pristine-state currents, forming, and set/reset operations. The 1T-1R devices studied in this work are integrated in IHP's 130 nm CMOS technology. The transistor has a gate length of 130 nm and a gate width of 1000 nm. The RRAM device is integrated between the Metal 2 and Metal 3 levels in the BEOL of the technology, consisting of TiN (150 nm) as the bottom and the top electrode, 3% Al-doped HfO2 as the switching layer, and Ti as the OEL. The devices investigated in this study are grouped by Ti OEL thickness: 7 nm, 9 nm, and 11 nm. For devices containing 7 nm Ti, the switching layer is varied to thicknesses of 3 nm, 4 nm, and 5 nm; for 9 nm Ti, the switching layer is varied to thicknesses of 4 nm and 5 nm; and for 11 nm Ti, the switching layer is 6 nm thick to have a consistent ratio of Ti/Al-doped HfO2 thicknesses in the devices. The variations of Ti/Al-doped HfO2 thickness ratio studied in this work are 2.3, 1.8 and 1.4.

Fig. 1 shows the Cumulative Distribution Function (CDF) of the pristine-state current measured at 1.5 V for the 1T-1R devices with different ratios of Ti/Al-doped HfO2 layer thicknesses. As shown in the figure, the pristine-state current is significantly influenced by the OEL/switching layer thickness ratio, with devices at a ratio of 2.3 (7/3 and 9/4) exhibiting higher pristine-state currents than other devices at ratios of 1.8 (7/4, 9/5, 11/6) and 1.4 (7/5). In Fig. 2, the CDF of forming voltages for the devices with pristine-state current below 1 µA are shown. The forming voltages also show a similar trend; lower forming voltages for devices with higher pristine-state currents, indicating that the switching properties are related to the ratio of OEL to switching layer thicknesses rather than to individual layer thicknesses.

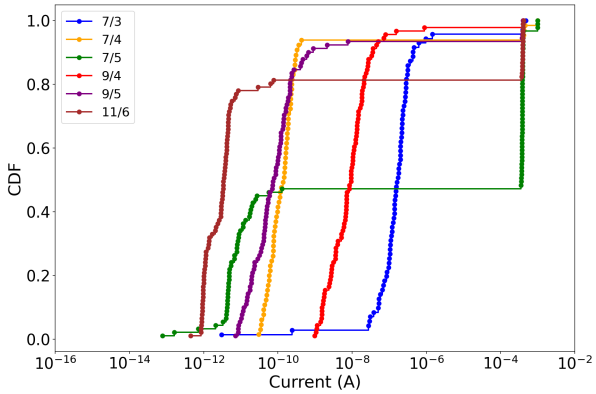


Figure 1. CDFs of pristine state current measured at 1.5 V for 1T-1R devices consisting of the different Ti:Al-doped HfO2 ratios mentioned above.

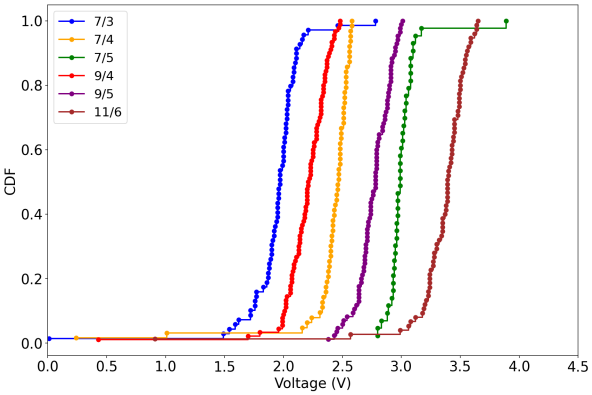


Figure 2. CDFs of forming voltages for the 1T-1R devices shown in Fig. 1 with pristine-state current below 1 µA (non-leaky devices).

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Insights into Voltage-Driven Degradation Processes in Hafnia-Based Memristive Devices

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Resistive-switching memory (RRAM) devices based on transition metal oxides are one of the most promising candidates for applications such as non-volatile memories, random number generation, and neuromorphic computing [1], due to their simple structure, low cost, low operating voltage, high density, scalability, high speed, and long endurance. However, switching variability and degradation phenomena under different operating conditions remain critical challenges that must be deeply understood to enable reliable device operation [2].

In this work, we investigate cycling variability and degradation in TiN/Ti/HfO_2/W memristive devices (Fig. 1 (a)) through controlled voltage-sweep with progressively increasing amplitudes [3]. Using three specifically designed experimental protocols that independently control the positive and negative voltage limits of the voltage ramp stimulus, we assess the evolution of the low-resistance state (LRS), high-resistance state (HRS), and the dynamics of SET and RESET transitions under repeated switching cycles.

The resulting I-V characteristics for each protocol are described as follows: (i) incremental variation of the positive voltage limit (VMAX-POS) every 100 cycles; (ii) incremental variation of the negative voltage limit (VMAX-NEG) every 100 cycles (Fig. 1 (b)); and (iii) alternation every 100 cycles between a fixed reference voltage range (V0-NEG, V0-POS) and a voltage range in which both VMAX-NEG and VMAX-POS are progressively increased (Fig. 2 (a)). These stress conditions induce degradation under distinct operating regimes, allowing the independent identification of the dominant degradation mechanisms governing device performance during cycling.

Since the voltage drop across Rseries can significantly affect the apparent switching voltages, its accurate extraction is essential for determining the intrinsic transition voltages. Rseries was estimated by correcting the measured I-V characteristics until a nearly vertical SET transition was obtained [4]. After removing Rseries contribution, the intrinsic SET (VTS) and RESET (VRS) voltages were extracted and analyzed. As an independent validation, Rseries was also determined from the dependence of VRESET on Rseries under different voltage stress conditions. The intersection of the resulting curves identifies the Rseries value that best accounts for the parasitic voltage drop, providing access to the intrinsic RESET transition voltage (VRS) of the memristive device (Fig. 2(b)) [5].

The experimental I-V characteristics were further reproduced using the Dynamical Memdiode Model (DMM) [6], which successfully captures the main features of the observed behavior and provides physical insight into the relationship between the model parameters and the different degradation phenomena observed during cycling (Fig. 1(b)).

These results reveal that VMAX-POS and VMAX-NEG primarily affect the resistance window through modifications of the HRS, likely associated with changes in the filament gap and defect distribution, while the switching thresholds remain largely unaffected, suggesting that the underlying switching mechanism is preserved.

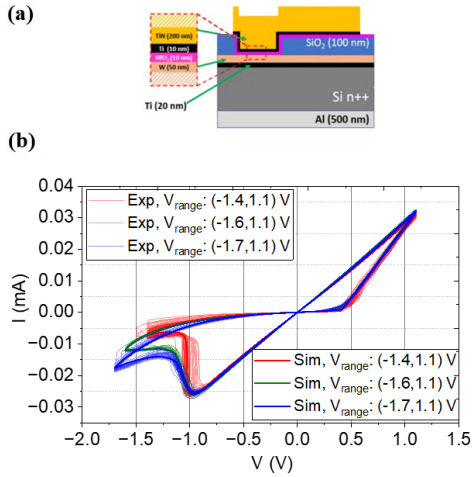


Figure 1. (a) Schematic cross-section (not to scale) of the studied TiN/Ti/HfO_2/W memristive cells. (b) Experimental and simulated I-V characteristics with VMAX-NEG increased by 100 mV every 100 cycles.

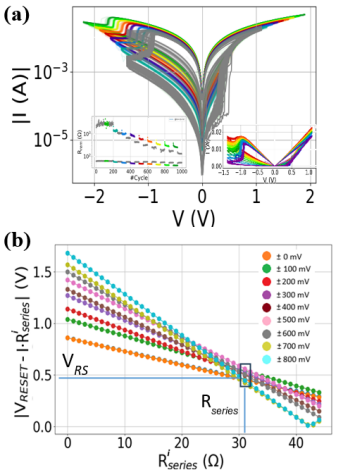


Figure 2. (a) I-V characteristics obtained by alternating, every 100 cycles, a fixed reference range (V0-NEG, V0-POS) (gray) with a voltage range where VMAX-NEG and VMAX-POS simultaneously increase by 100 mV (color-scale). Left inset: LRS and HRS evolution over cycling. Right inset: I-V curves measured at (V0-NEG, V0-POS) after cycling. (b) Rseries estimation method: VRESET is determined as a function of Rseries under the different stress conditions. The intersection point defines the most representative VRS-Rseries value.

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High-Temperature Retention and Degradation Mechanisms of Multilevel Conductive-Metal-Oxide/HfO_x ReRAM

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Filamentary oxide-based resistive random-access memory (ReRAM) is a leading candidate for embedded non-volatile storage and analog in-memory computing, owing to its simple two-terminal structure, low operating voltage, and CMOS back-end-of-line (BEOL) compatibility [1]. Among the various material stacks reported to date, bilayer conductive-metal-oxide (CMO)/HfO_x devices have demonstrated particularly attractive analog switching characteristics, including sub-1.5 V operation, more than 32 stable conductance states, and a unified on-chip training and inference platform [2].

These properties make the CMO/HfO_x stack uniquely suited for applications that encode information across a continuum of conductance levels rather than in binary states. However, the thermal stability of such intermediate analog states remains largely unexplored. Unlike binary switching, where failure is defined by the loss of margin between high- and low-resistance states [5], analog retention is governed by gradual oxygen-vacancy redistribution within the CMO layer and trap-assisted conduction [4] , mechanisms that conventional digital retention metrics are not equipped to capture. With demanding applications such as automotive systems requiring stable operation across −40 °C to 150 °C (AEC-Q100 Grade 0) [3], a dedicated thermal characterization of analog CMO/HfO_x ReRAM is critically needed.

In this work, we present a systematic high-temperature retention study of multilevel CMO/HfO_x ReRAM devices integrated in a 1-transistor–1-ReRAM (1T1R) configuration (Fig. 1). Four distinct resistive states: HRS, LRS, and two intermediate states (IRS1, IRS2) are programmed using an identical-pulse closed-loop scheme [2]. Then subjected to step-stress accelerated life testing (SS-ALT) at 85 °C, 110 °C, and 130 °C over successive 24-hour baking cycles, with devices reprogrammed between steps. This cumulative testing approach was adopted to better replicate the conditions experienced by ReRAM devices in real-world applications.

Two distinct degradation regimes are identified and decoupled: a reversible, instantaneous resistance shift consistent with trap-assisted conduction through the CMO layer, and an irreversible, time-dependent retention degradation. The latter is governed by two competing mechanisms: a gradual resistance increase from radial oxygen-vacancy diffusion away from the filament core, and an abrupt, permanent resistance drop from directional vacancy migration toward the active electrode. Notably, extended high-temperature exposure at is found to trigger an annealing effect at the HfO_x/CMO interface, substantially improving subsequent retention performance. Activation energies extracted via Arrhenius analysis (∼1.5 eV) are state-independent, consistent with a unified vacancy-diffusion process. An empirical SPICE compact model, incorporating a time- and temperature-dependent term describing oxygen-vacancy evolution in the CMO dome [4], reproduces the observed retention kinetics across all tested states and temperatures up to failure, providing a predictive tool for lifetime extrapolation (Fig. 2).

These results provide new physical insight into the thermal limits of analog ReRAM operation and establish a methodology for assessing multilevel retention reliability beyond conventional binary criteria, a critical step toward deploying analog ReRAM in thermally demanding environments.

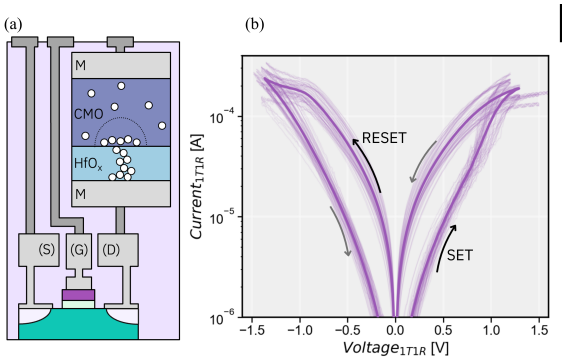


Figure 1. (a) Schematic cross-section of the CMO/HfOx-based 1T1R ReRAM cell integrated in the CMOS BEOL, illustrating the source (S), gate (G), and drain (D) terminals of the access transistor, and the oxygen vacancies distribution within the HfOx and CMO layers forming the conductive filament and dome, respectively. (b) Quasi-static I-V characteristics of the 1T1R cell over 5 cycles per device (light curves), with the average curve highlighted in bold.

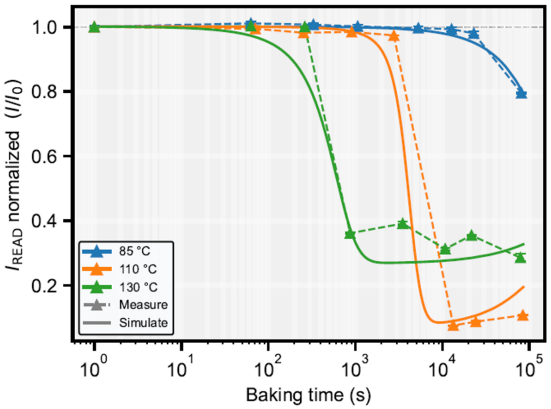


Figure 2. Normalized read current, IREAD/I0, as a function of baking time at 85, 110, and 130°C. Dashed lines with markers correspond to the experimental data, while solid lines represent the simulated fit obtained with the proposed empirical model.

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Talks

Analog Computing

Emerging Analog Memories as Knobs for Multi-Scale Neural System Design

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Emerging analog memories are often viewed primarily as dense, nonvolatile storage elements for synaptic weights or as devices for accelerating matrix-vector multiplication. In this talk, I will argue for a broader perspective: emerging memories can act as physical knobs that tune the structure and dynamics of neural systems across multiple spatial and temporal scales.

At the synaptic scale, analog memory can encode weights, local plasticity, and short- or long-term state. At the neuronal scale, device dynamics can contribute to adaptation, gating, excitability, and multi-timescale integration. At the dendritic scale, memory elements can support compartmentalized processing, delays, and nonlinear integration. At the network scale, embedded nonvolatile memories can enable reconfigurable local connectivity, in-memory routing, and sparse communication patterns that reduce costly data movement. In this view, emerging memories are not only passive storage media, but active ingredients for shaping the computational morphology of artificial neural systems.

I will discuss examples from our recent work on memory-centric neuromorphic architectures, including dendritic processing with resistive memory, in-memory routing for small-world connectivity, and hardware-aware learning methods that incorporate locality, sparsity, delays, and temporal hierarchy as algorithmic priors. These examples illustrate how device properties can be lifted into architectural and algorithmic design choices, and how neural network structure can in turn be adapted to the physical constraints of the substrate.

The central message is that the opportunity for emerging analog memories lies not only in improving density or energy efficiency at a single layer of the stack, but in enabling co-design across devices, circuits, architectures, learning algorithms, and applications. Building future intelligent systems will require treating memory, communication, and time as coupled design variables across multiple spatial and temporal scales.

Performance-Reliability Co-Optimization of TrioN(3N0C) Synaptic Memory for Analog AI Acceleration

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Analog compute-in-memory(aCIM) based on cross-point arrays has emerged as a promising hardware platform for deep neural network inference and training, as it can perform massively parallel matrix-vector multiplication for forward propagation, as well as backward propagation and outer-product weight updates directly inside memory arrays. Among various memory concepts as cross-point elements, capacitor-based synapses have attracted attention as they can provide fast, gradual, and symmetric analog updates based on transistor- controlled precise charge modulation. However, conventional CMOS-based cell concept faced limitations in scaling, retention, and circuit complexity due to explicit capacitors, multiple devices, and PMOS/NMOS integration[1,2]. To address these challenges, TrioN(3N0C) has been studied as a capacitor-less IGZO-based synaptic memory concept that exploits the ultralow off-leakage and parasitic capacitance of oxide transistors[3]. TrioN has demonstrated strong potential as an ideal analog synaptic device by achieving highly symmetric conductance modulation, large on/off ratio, and ultrafast 10ns switching, while addressing the scaling and retention limitations of conventional capacitor-based cells. Using only three IGZO transistors, TrioN stores analog weights at a floating storage node formed by overlap capacitance without requiring explicit capacitor or PMOS transistor. In a perspective of analog AI accelerator, TrioN offers and architecture-level advantage by enabling fully-parallel weight update without cell-to-cell interference in cross-point arrays. The two series-connected write transistors act as an AND-type selector allowing programming only at targeted cells, and further supports an efficient 2-cycle stochastic update scheme that halves the update sequence of conventional 4-cycle schemes, thereby improving on-chip training efficiency. Meanwhile, IGZO-based charge-storage memories are strongly affected by oxygen vacancy related defects such as channel–dielectric interface traps, hysteresis, and bias-stress instability. Therefore, controlling these defect states is essential, as emphasized in oxide-transistor based 2T0C DRAM research. We developed process-engineering strategies to optimize contact formation, thermal annealing, and passivation to suppress trap-related instability[4,5]. We successfully demonstrated performance–reliability co-optimized IGZO transistors with small hysteresis(∼70mV), robust positive/negative bias-stress stability, enhanced on-current (x2), and ultralow off-leakage(6.12aA/μm) . Enabled by these transistor-level improvements, our performance-reliability co-optimized TrioN cell achieves near-ideal symmetric switching with a large on/off ratio exceeding 1,000 even with 10 ns switching, >4 bit multilevel programmability, reproducible endurance over 6×10^3 pulses, and long retention with ΔVSN below 50 mV[6]. Furthermore, to evaluate its potential as an analog AI accelerator, a 2K IGZO 3T0C cross-point array was experimentally demonstrated for the first time through array-level conductance modulation. Device–algorithm co-optimization highlights the strong potential of TrioN for practical analog AI training. Using measured 3N0C characteristics, asymmetry-aware Tiki-Taka training achieves 97.7% and 98.5% MNIST accuracy for MLP and LeNet-5, respectively. Furthermore, array-level linear regression is experimentally demonstrated, and hardware-aware training with TrioN-based analog layers recovers MobileBERT SST-2 accuracy from 41.86% to 89.11%, extending TrioN from a most compact capacitance-based synaptic device to an algorithm-compatible memory candidate. These results indicate

that further advances in TrioN-based analog AI hardware will rely on simultaneous optimization across device performance, on-chip in-situ training, and algorithm compatibility to achieve low-power, accurate, and efficient inference and training.

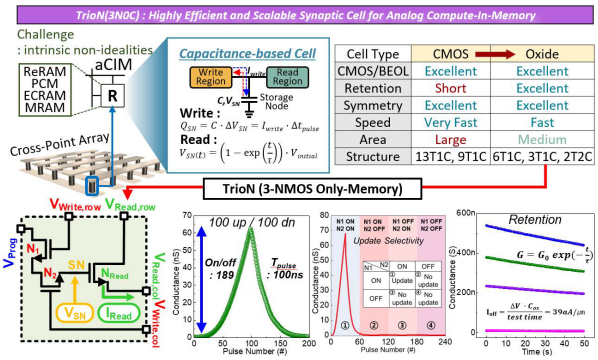


Figure 1. Introduction of TrioN concept and ideal synaptic characteristics. Cross-point-array-based aCIM with decoupled write/read operations, enabling transistor-controlled analog weight modulation, parallel matrix–vector multiplication, and stochastic weight update. TrioN shows symmetric analog switching with a large on/off ratio, fast 100 ns update, AND-type selective update, and retention enabled by extremely low off-leakage.

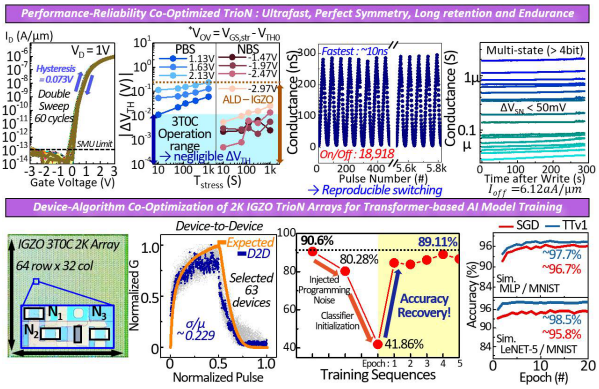


Figure 2. Performance–reliability co-optimized TrioN for analog AI training. Process-engineered IGZO transistors with small hysteresis, PBS/NBS stability, enhanced on-current, and ultralow off-leakage. Improved TrioN performance with 10 ns switching, >4-bit operation, reproducible endurance, and long retention. 2K IGZO 3T0C array and Device–algorithm co-optimization validating MNIST training, array-level linear regression, and MobileBERT SST-2 recovery.

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Analog Conductance Modulation in Percolative $Ge_2Sb_2Te_5$ Pathways Confined within a HfO_2 Nanoparticle Matrix

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Phase-change memory (PCM) has attracted considerable attention for both nonvolatile memory and neuromorphic computing applications owing to its nonvolatile resistance switching, large resistance contrast, fast operation, and capability for multilevel conductance modulation [1,2]. PCM stores information through reversible transitions between highly resistive amorphous and conductive crystalline phases, allowing memory states and synaptic weights to be retained without continuous power or periodic refresh [1,2]. However, conventional PCM devices often exhibit abrupt conductance changes because the size and location of the active phase-change volume are difficult to control precisely. Spatial confinement of the GST active volume is therefore expected to enable more gradual and controllable conductance modulation [3].

In this work, we investigate the analog conductance modulation characteristics of a PCM device incorporating a nanocomposite formed by alternately stacking HfO_2 nanoparticles and $Ge_2Sb_2Te_5$ (GST) nanoparticles. This architecture is designed to promote the formation of percolative GST pathways while spatially confining the GST active regions within an HfO_2 nanoparticle matrix. HRTEM analysis confirmed the formation of discrete GST and HfO_2 nanoparticles, with the GST nanoparticles exhibiting diameters of approximately 5–6 nm. The insulating HfO_2 nanoparticles restrict the effective phase-change volume of GST, thereby facilitating reversible SET and RESET conductance modulation.

During voltage sweeps using a source-measure unit, the device exhibited RESET-like behavior at a relatively low voltage of approximately 1.8 V, followed by gradual conductance reduction under subsequent identical sweeps. Pulse measurements demonstrated stable conductance modulation over approximately 2,500 programming pulses. Potentiation was induced using 2.9 V pulses with a width of 300 ns, whereas depression was achieved using 3.2 V pulses with a width of 20 ns. The device also exhibited eight distinguishable conductance states, corresponding to 3-bit multilevel storage, with read-current levels of approximately 268, 374, 435, 485, 500, 521, 551, and 568 μA. These programmed states were maintained for 600 s with an average retention ratio of approximately 90%, indicating reliable multilevel weight storage.

Compared to conventional PCM devices with a planar GST layer, the proposed nanoparticle-composite device exhibited more gradual conductance modulation at a lower operating voltage, despite its relatively large contact diameter of 50 μm [4,5]. These results suggest that the GST/HfO_2 nanoparticle composite provides a promising device architecture for confined phase-change operation and multilevel synaptic weight modulation.

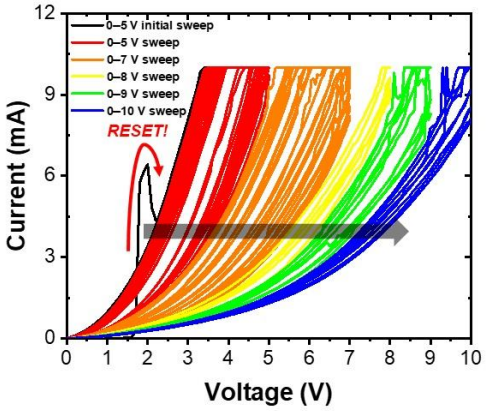


Figure 1. I–V characteristics obtained from sequential voltage sweeps of 0–5, 0–7, 0–8, 0–9, and 0–10 V.

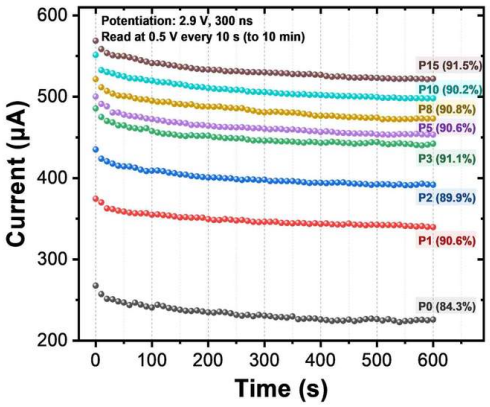


Figure 2. Retention of distinguishable multilevel conductance states programmed with different pulse numbers for 600 s.

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Wafer-Scale Hexagonal Boron Nitride Memristors with Reliable Analog Switching

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Wafer-scale hexagonal boron nitride (h-BN) memristors are attractive candidates for neuromorphic hardware owing to the atomically smooth surface, large breakdown field[1], chemical stability[2], and compatibility with scalable chemical vapor deposition[3]. However, previously reported h-BN memristors predominantly exhibit threshold-driven filamentary switching, in which positive feedback during filament formation results in abrupt conductance changes that are unsuitable for on-chip learning requiring gradual and reproducible weight updates.

Here, we demonstrate intrinsic analog switching in wafer-scale h-BN memristors through post-growth Ar ion implantation. MOCVD-grown h-BN films on Si substrates were subjected to controlled ion implantation, which simultaneously introduces defects into the h-BN layer and amorphizes the underlying Si. Electrical measurements reveal a systematic transition from abrupt filamentary switching in pristine devices to continuous analog conductance modulation with increasing implantation dose. Spectroscopic and microscopic analyses indicate that switching remains governed by defect-mediated transport within the h-BN layer, while the amorphized Si acts as an interfacial modifier that introduces additional series resistance and suppresses the positive feedback responsible for runaway filament growth. The implantation-induced defects further establish a spatially distributed trap network, enabling gradual conductance evolution under identical programming pulses without external compliance control or closed-loop programming schemes.

The resulting devices exhibit stable multilevel states spanning more than three orders of magnitude in current and voltage-tunable potentiation and depression characteristics. Device-to-device variation remains low, with an average coefficient of variation of only 2.7% across multiple devices Furthermore, the analog states are highly reproducible and remain stable over 50k programming pulses, demonstrating the robustness required for neuromorphic computing applications.

Because both MOCVD growth and ion implantation are industry-compatible wafer-scale processes performed directly on the target substrate without any transfer of two-dimensional materials, this work establishes implantation-based heterostructure engineering as a scalable route toward intrinsically analog operation in two-dimensional memristors and provides a practical pathway for implementing reliable on-chip learning hardware based on h-BN.

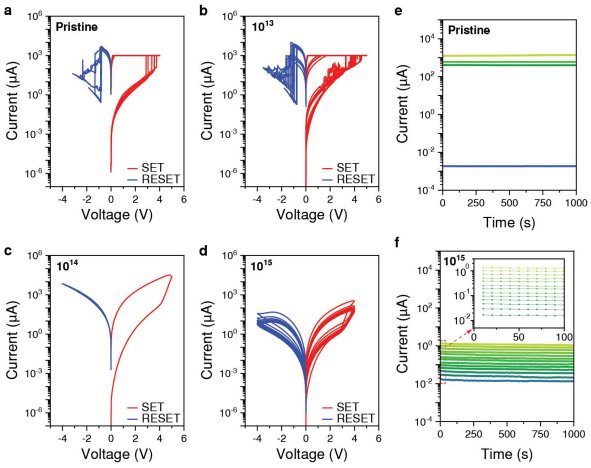


Figure 1. (a–d) DC I–V characteristics of representative devices under increasing 60 keV Ar ion dose: (a) pristine, (b) 10^{13} ions·cm^(-2), (c) 10^{14} ions·cm^(-2), and (d) 10^{15} ions·cm(-2). The pristine and 10^{13} devices exhibit sharp threshold-driven transitions, the 10^{14} device shows gradual modulation but incomplete RESET, and the 10^{15} device shows fully hysteretic analog switching in both polarities. (e) Multilevel retention of a pristine device. Three discrete states programmed using compliance currents of 10^(-4), 10^(-3), and 10^(-2) A during SET are retained for more than 1000 s at a read voltage of 0.2 V. (f) Multilevel retention of a 10^{15} implanted device. Sixteen distinct conductance states at a read voltage of 0.2 V, are retained for more than 1000 s without any current compliance during programming.

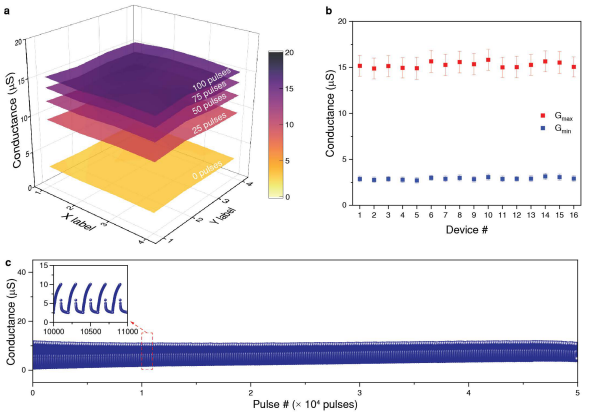


Figure 2. 16 nominally identical devices were selected at random across the wafer and subjected to an identical pulse scheme consisting of 100 potentiation pulses (V_P = 3.4 V, 10 ms) followed by 100 depression pulses (V_D = -2.7 V, 10 ms) per cycle, with a read pulse (V_R = 0.2 V) applied between every programming pulse. Statistics in (a) and (b) are extracted from 25 stable cycles per device (cycles 6 to 30). (a) A 4 × 4 conductance grid of the 16 devices at five characteristic states within averaged P–D cycles: G_min (0 pulses), and after 25, 50, 75, and 100 potentiation pulses (G_max). (b) Per-device G_max (red) and G_min (blue) for the 16 devices. Square symbols denote the mean value over the 25 stable cycles and error bars denote the cycle-to-cycle standard deviation within each device. The mean G_max is 15.27 μS (device-to-device standard deviation 0.30 μS, CV = 1.97 %), and the mean G_min is 2.91 μS (standard deviation 0.12 μS, CV = 3.96 %). (c) Long-term cycling of a representative device under continuous P–D operation. G_max and G_min envelopes remain within their initial windows throughout 50k programming pulses (250 P–D cycles). Inset image shows representative cycles near 10k pulses, confirming that the analog P–D response is preserved during cycling.

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Talks

Organic Memristors

Memristors with Organic Self-Assembled Monolayers

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Functionalized self-assembled monolayers (SAMs) can be used as active components in electronics and spintronics devices. In particular, SAMs composed of dipolar, conformationally flexible phosphonic acids enable electrically switchable tunnel junctions with memristive characteristics [1]. The performance of such organic memristive devices is comparable to that of their state-of-the-art inorganic counterparts. The big advantage of organic systems is their intrinsic functional versatility: a rather complex property profile can be easily designed into the individual component molecules. A potential challenge of many SAM systems - thermal stability - was resolved by using thermally and chemically robust phosphonic acids as anchoring groups which are compatible with oxide and nitride substrate materials common in electronics industry.

Another class of functional SAMs is composed of chiral compounds, such as binaphthol phosphates (BNP), which can act as electron spin filters [2]. Phenomena around the interaction between electrons of different spin and chiral thin films are known as the chirality-induced spin selectivity (CISS) effect. The CISS effect of chiral SAMs can be utilized for simplified spintronics devices where the SAM replaces the pinned magnetic layer.

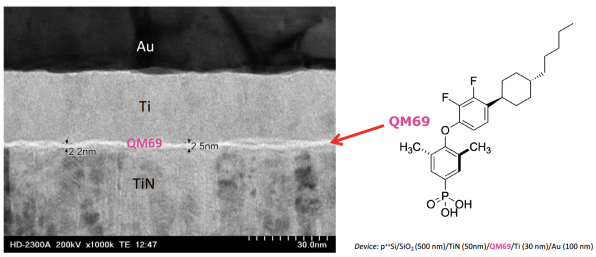


Figure 1. Tunnel junction based on a organic monolayer of a phosphonic acid with a electrically switchable dipole moment.

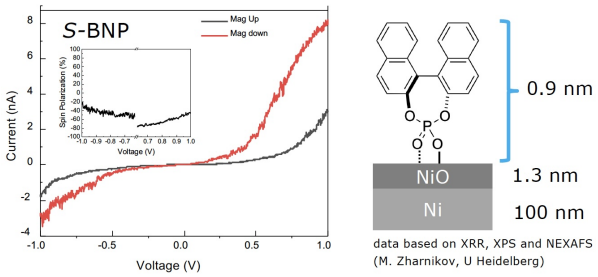


Figure 2. Dependence of tunnel current on the magnetization of the ferromagnetic nickel substrate.

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Memristive and neuromorphic properties of CdIn2S4-based devices driven by metastable defect complexes

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Memristive technologies are currently advancing towards greater stability and lower energy consumption [1]. In this context, defect-driven electronic switching can provide an alternative to existing filamentary and ion-migration-driven mechanisms. Herein, we present the memory and neuromorphic properties of Mo/CdIn2S4/AZO–Al double-barrier heterostructures, in which metastable negative-U defect complexes govern resistive switching and interact with interface barriers [2]. The operation of the devices can be interpreted within the broader framework of defect-level switching (DLS), which is currently gaining increasing interest [3]. In this approach, changes in conductivity of the device arise from charge trapping and detrapping at immobile metastable defects, rather than from charge or mass transport. In CdIn2S4, sulfur vacancy plus antisite type defect complexes exhibit multiple charge states and large lattice relaxation, enabling persistent transitions between deep and shallow configurations. These defect transitions can dynamically modulate the spatial distribution of charge and, consequently, the band bending at the interfaces. These processes result in the device behaviour as two coupled rectifying junctions with history-dependent space-charge-region widths, leading to reversible switching between distinct conductive regimes and, therefore, to the emergence of the pinched hysteresis loop (PHL). Such a description is consistent with the contemporary defect physics framework developed for II–VI and chalcopyrite semiconductors (i.e., the Lany–Zunger model [4], and related works [5,6]), in which metastable defect complexes control persistent photoconductivity and bias-induced persistent states in semiconductor thin films.

We developed a physical model that associates metastable defect kinetics and charge redistribution with the resulting modulation of interface barriers of the device. In this approach, the switching dynamics of the device are inherently time-dependent and governed by the evolution of the spatial distribution of metastable defects. Such framework can consistently explain the observed pinched hysteresis loops, their non-transversal form, and the devices' dependence on excitation conditions, including pulse frequency and history. The model can be further developed to connect the memristive properties with the internal state variable of the device.

Beyond standard electrical characterisation, including I-V characteristics, we evaluated the devices using the modified Di Ventra–Pershin test for ideal memristors [7], demonstrating that, over a certain range of stimulation, the devices fulfil the memristor criterion. Moreover, the devices demonstrate key neuromorphic functionalities, including electrical gradual potentiation, Paired-Pulse Facilitation (PPF), and optically induced plasticity enabled by persistent photoconductivity. The latter arises from optically driven transitions in defect charge states, providing an additional degree of control over the internal state by applying optical pulses. Such combined electrical and optical tunability is particularly attractive for neuromorphic and in-memory computing systems. The presented results position CdIn2S4, as well as a broader class of defect-engineered semiconductor materials rich in metastable defects, as potential sources of alternative physical mechanism for tunable non-filamentary switching and neuromorphic functionality.

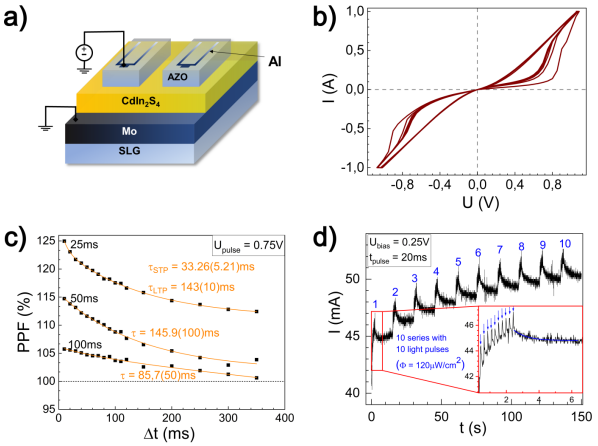


Figure 1. Device structure and operation under electrical and optical stimuli. a) Structure of the device; b) I-V characteristics, showing PHL, c) PPF performance under variable pulse duration; d) 10 epochs of optical pulse potentiation.

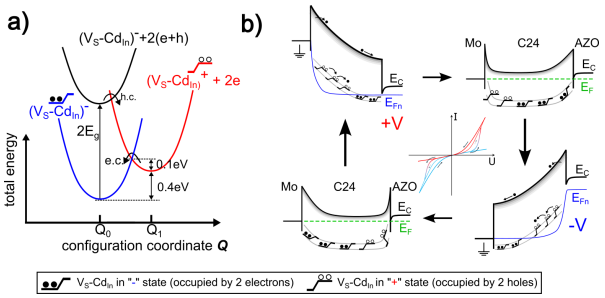


Figure 2. Principle of opeation of metastable defect based memory. a) configuration coordinate diagram of the metastable defect complex in CdIn2S4; b) Principle of devices' operation based on metastable defect-level switching.

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A Highly Stable Multimodal Perovskite Heterojunction Memristor Enabling In-Memory Perception

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Advancements in computing architectures have evolved from near-sensor processing toward in-sensor computing, culminating in multimodal in-memory computing where sensing, storage, and computation coexist within a single platform. This approach reduces the energy and latency penalties of von Neumann architecture by performing computation directly within memory devices. Although perovskite memristors show promising switching and optoelectronic properties, their susceptibility to degradation under humidity, temperature variation, repeated switching, and light exposure remains a key challenge, with systematic evaluation under prolonged extreme conditions rarely reported.

Here, for the first time, we report a robust VOx-encapsulated perovskite heterojunction memristor engineered for multimodal in-memory sensing and neuromorphic operation, demonstrating excellent electrical stability, environmental resilience, and multisensory reconfigurability.

The device structure comprises a Cu/VOx/PVK/Pt stack, where the VOx layer serves as both a protective encapsulation and functional interface. The device exhibits extremely stable bipolar resistive switching with well-defined SET and RESET transitions. AC endurance measurements confirm reliable operation over 10 million cycles, with negligible variation between high-resistance state (HRS) and low-resistance state (LRS). LRS retention remains stable up to 10^4 s under a 0.1 V read bias, and uniform switching voltage distributions across multiple devices confirm good device-to-device consistency. STEM-EDS mapping of fresh devices confirms structural composition and well-defined interfaces.

To evaluate environmental robustness, the memristor was subjected to extreme temperature and humidity conditions over a period exceeding 1 year. Temperature was varied from cryogenic conditions ($\sim$100 K) up to 448 K. The threshold voltage (VTH) shows systematic modulation with temperature, indicating tunable switching dynamics without device failure. Even after thermal stress, the device maintains stable LRS retention, DC endurance over 10^4 cycles, and AC endurance of 10 million cycles therefore demonstrating that VOx encapsulation effectively mitigates thermal-induced degradation while preserving functional performance.

Humidity resilience was assessed at relative humidity (RH) levels of 1% (dry), 60% (ambient), and 95% (extremely humid). Modulation of I–V characteristics and VTH under varying RH conditions highlights the capability for in-memory humidity sensing. After extreme humidity exposure, the device demonstrates recoverability through controlled dehumidification and vacuum degassing. Post-stress STEM-EDS mapping confirms the VOx encapsulation layer remains intact with minimal diffusion or structural damage after more than one year. While Cu diffusion is observed across layers, this is consistent with its active role in filamentary switching and does not compromise performance.

Beyond environmental sensing, the device exhibits optoelectronic synaptic behavior under broad-wavelength optical stimulation (405, 465, 532, and 635 nm). Under 465 nm and 532 nm illumination, stable post-synaptic current (PSC) enhancement is observed, tunable by pulse number, width, and laser power. At 405 nm, PSC continues to rise transiently after illumination ceases, suggesting photo-carrier trapping and defect-assisted recombination dynamics. Notably, 635 nm illumination produces a sharp PSC drop below baseline upon light removal causing negative retention therefore enabling both excitatory and inhibitory synaptic responses within a single device.

Overall, the VOx-encapsulated perovskite memristor demonstrates multimodal sensing, long-term en-

vironmental stability, high endurance, and reconfigurable synaptic plasticity, positioning it as a strong candidate for next-generation in-memory computing systems.

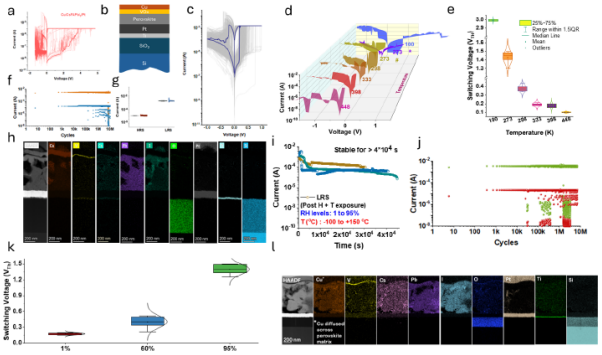


Figure 1. (a) I-V curve of Cu/Perovskite/Pt, (b) schematic, (c) I-V curve of Cu/VOX/Perovskite/Pt. (d-e) Temp-dependent VTH (100-448K). (f-g) AC endurance (fresh device). (h) STEM-EDS of fresh device. (i) LRS retention (>4x10^{4}s), (j) AC endurance (post T measurements). (k) VTH at 1-95% RH. (l) Post-stress STEM-EDS confirming VOx integrity.

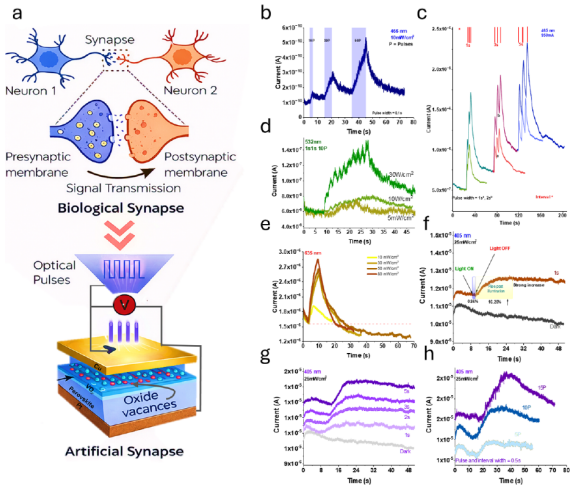


Figure 2. (a) I-V curve of Cu/Perovskite/Pt, (b) schematic, (c) I-V curve of Cu/VOX/Perovskite/Pt. (d-e) Temp-dependent VTH (100-448K). (f-g) AC endurance (fresh device). (h) STEM-EDS of fresh device. (i) LRS retention (>4x10^{4}s), (j) AC endurance (post T measurements). (k) VTH at 1-95% RH. (l) Post-stress STEM-EDS confirming VOx integrity.

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Deterministic Control of Neuromorphic Behavior in SI-ATRP Engineered Polymer Brush Memristors

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As neuromorphic computing transitions from single-device demonstrations to large-scale hardware neural networks, a critical bottleneck remains the stochastic nature of resistive switching and the lack of deterministic design rules. While traditional inorganic memristors often suffer from filamentary variability, organic material systems offer unparalleled chemical tunability. However, their performance is frequently compromised by structural disorder. To address this challenge, the precise engineering of macromolecular architectures offers a powerful ”bottom-up” pathway to eliminate disorder and develop highly tunable molecular memristors with nanometer-scale precision.

In this study, we present a robust platform based on poly(glycidyl methacrylate) (PGMA) brushes synthesized via surface-initiated Atom Transfer Radical Polymerization (SI-ATRP) on rigid indium tin oxide (ITO) substrates. To systematically modulate the electronic environment and charge transport properties, the reactive epoxide rings of the PGMA backbone underwent post-polymerization modification. We introduce a ”molecular dilution” strategy where the density of redox-active charge-trapping centers is precisely tuned by functionalizing the brushes with varying ratios of aminoferrocene (redox-active) and hexylamine (aliphatic/passive), ranging from fully functionalized (100% aminoferrocene) to systematically diluted matrices (e.g., 75% aminoferrocene / 25% hexylamine). The memristive devices were finalized by evaporating top gold (Au) electrodes to form an ITO/polymer brush/Au architecture.

The successful grafting, chemical composition, and precise control over film stoichiometry were comprehensively verified using Fourier-Transform Infrared Spectroscopy (FTIR) and X-ray Photoelectron Spectroscopy (XPS). Atomic Force Microscopy (AFM) and Conductive AFM (C-AFM) were utilized to map surface morphology and local current pathways, providing critical insights into the nanoscale resistive switching mechanisms and device homogeneity.

Macroscopic electrical characterization via cyclic voltammetry (CV) confirmed stable and reproducible memristive behavior across the entire dilution series. To thoroughly understand the transport kinetics and switching reliability, temperature-dependent measurements and noise characterization were conducted. Furthermore, the devices exhibited robust synaptic characteristics, including well-defined potentiation and depression behavior. Leveraging these experimental synaptic weights, artificial neural network simulations demonstrated high accuracy in pattern recognition tasks. Finally, theoretical modeling of the device structure was performed to complement experimental findings and corroborate the underlying switching mechanisms. This work establishes clear molecular structure-property relationships in functionalized polymer brush systems, offering viable design rules for tailorable organic hardware in next-generation neuromorphic computing.

A Self-powered Optoelectronic In-sensor PUF Based on Halide Perovskites

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In the rapidly evolving landscape of the Internet of Things (IoT) and the increasing reliance on data-driven technologies, implementing robust security measures has become essential. In particular, the authentication of goods and verification of personal identities require innovation to reduce the risk of counterfeiting. One of the ways to achieve this is to leverage the inherent variability between sensors induced during the manufacturing process which can be used to generate unique and unpredictable input and output combinations. Perovskite thin films fabricated through solution-processing methods show spatial variation in optical response owing to thickness and film quality differences across the area of the thin film. Based on this premise, single-device optical physically unclonable functions (PUF) built from halide perovskite photovoltaics based on methylammonium lead bromide as well as on methylammonium lead iodide have been introduced. The fundamental principle of a PUF is to take an input challenge and generate a unique and reliable response based on the inherent variations of the device. A single PUF can accept multiple challenges and produce unique responses for each one. The conventional implementations of PUFs require fabrication through complex cleanroom processes on rigid substrates which can limit their applications. Solution-processing techniques are a cost-friendly method of fabricating PUFs, and are also compatible with flexible substrates and printing technologies.

Optical PUFs, which employ optical signals as the challenge, demonstrate better security and increased stability to environmental conditions. While most optical PUFs use photoluminescent or fluorescent patterns as unique responses, this work uses a much more convenient method to obtain PUF responses in the form of open-circuit voltage. The multi-bit PUF is generated using 4-bit optical pulse trains, which generate unique output voltages due to slow photovoltage decay of the perovskite devices. The photovoltaic architecture and superior light sensitivity offer a unique approach for a self-powered in-sensor PUF, as no bias voltage is required to elicit a response from the perovskite PUF. Owing to the complex interplay of ionic and electronic processes in halide perovskites and manufacturing variations, each device responds uniquely, but reproducibly, to varying optical inputs. As a result, each device provides multiple untraceable encryption keys to implement a single device multibit PUF. A comparison between the PUFs based on the different halide perovskites has been drawn, showing better performance for the MAPbBr3 PUF. Hysteresis index measurements at different sweep rates and galvanostatic measurements were employed to understand the mechanism due to which the MAPbBr3-based device is a better-performing PUF its MAPbI3-based counterpart. The MAPbBr3-based PUF shows a good uniformity of 46.52% and a peak around 50% for bit-aliasing frequency. It also shows remarkable reliability, as indicated by a minimal coefficient of variance of 1–2% in open-circuit voltage across 10^5 cycles. Our multibit optoelectronic perovskite PUF with high reliability and good uniformity presents a safe and reliable security measure against theft and counterfeiting. Furthermore, its reusability lends itself to applications like multistage verification, providing an in-sensor and self-powered method to track goods across different stages throughout production and transportation of goods.

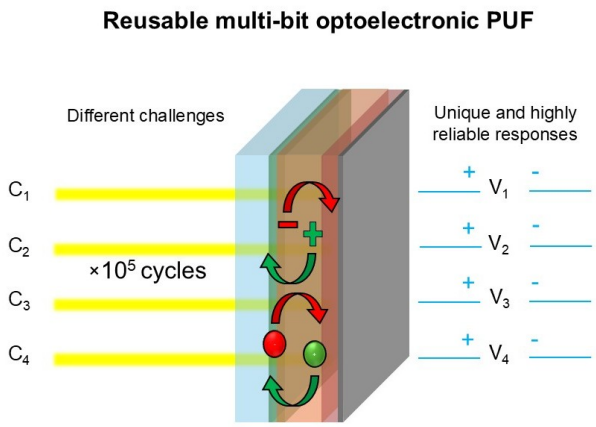


Figure 1. A schematic of the functioning of a multi-bit optoelectronic PUF developed using a perovskite solar cell device

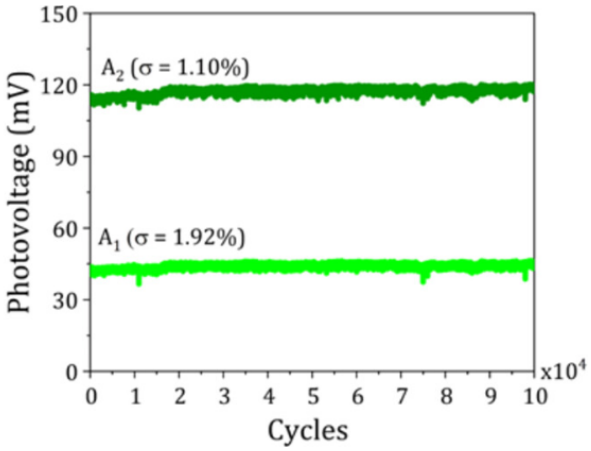


Figure 2. Endurance of the developed perovskite PUF, showing state-of-the-art reliability over 10^5 cycles for two successive optical pulses

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Soft reconfigurable self-assembled materials for embodied computing

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In pursuing machine intelligence comparable to biological systems, one often overlooks the crucial role of the body in enabling efficient data processing. In contrast to silicon-based architectures, it is well known how biological organisms exploit the intrinsic physical properties of their morphology and materials to support sensing, actuation, and low-energy information processing. This perspective has motivated the development of embodied intelligent systems, where computation emerges from the physical interactions between materials and the environment. Drawing inspiration from these principles, artificial systems can rise the challenge to integrate sensing, actuation, and control systems directly within their materials, improving processing efficiency and autonomy, in an unconventional, albeit biologically-inspired strategy.

Here we demonstrate how soft nanocomposite materials, based on metallic cluster-assembled thin films implanted in polydimethylsiloxane (PDMS) substrate[1] and deposited on paper, can perform reliable processing, in ambient environmental conditions. We exploit the nonlinear electrical behaviour of the self-assembled nanostructured network to implement soft variable resistances and reconfigurable nonlinear threshold logic gates[2], able to adapt to mechanical stimuli. Furthermore, we investigate how environmental factors, like humidity and temperature, influence the resistive switching and computational capabilities of these nanocomposites,[3] with the goal of developing multifunctional materials that combine sensing and computation on the same soft substrate to support adaptive, energy-efficient embodied intelligence for edge computing devices. In particular, we demonstrate the advantages resulting from the use of these resistive switching devices to classify time series and analog signals in real-time, requiring limited datasets for training and limited memory storage, as an edge application characterized by higher interpretability and accuracy with respect to artificial neural networks.[4]

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Talks

Reservoir Computing

Iontronic and Spintronic Reservoirs: Toward In-Materia Sensor Computing

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Artificial neural networks (ANNs) have achieved excellent learning, classification, and inference capabilities, approaching and in some cases surpassing those of natural intelligence. However, their energy consumption remains far higher than that of the human brain, motivating alternative computing paradigms for energy-efficient processing of sensory and time-series data. Physical reservoir computing (PRC) is a promising approach because it exploits the nonlinear dynamics of a physical reservoir (a material or device that responds dynamically to input signals), thereby reducing the computational resources needed for temporal information processing.

In this invited talk, I will present our recent progress in high-performance PRC devices based on iontronic and spintronic phenomena, and discuss their potential for in-materia sensor computing. Here, in-materia sensor computing denotes a materials-enabled in-/near-sensor computing paradigm in which intrinsic material dynamics, such as ion-electron coupling, mechanical-to-electrical transduction, and spin-wave interference, are exploited as computational resources for sensing, memory, preprocessing, and inference.

One representative iontronic platform is an ion-gating reservoir (IGR) that utilizes ion-electron coupled dynamics near a solid electric double layer at the diamond/Li+ solid-electrolyte interface [1]. The edge-of-chaos state of this reservoir yields optimal computational capacity. We have also demonstrated an IGR consisting of graphene and ion gel, which exhibits an exceptionally broad response range from 20 Hz to 1 MHz while maintaining high information-processing capacity and adaptability across multiple time scales (Fig. 1) [2]. This IGR achieved deep-learning-level accuracy in chaotic time-series prediction while reducing computational resource requirements to 1/100 of those needed by deep learning. In parallel, we have developed a magnonic PRC device that exploits the high-speed nonlinear dynamics of interfering spin waves in a ferrimagnetic Y3Fe5O12 single crystal [3].

Finally, I will discuss how these reservoirs can be integrated with sensors for real-time in-materia sensor computing. Examples include a spoken-digit recognition system that directly processes throat vibrations by combining a π-gel-electret mechano-electric generator sensor with a multi-channel ion-gel/graphene IGR, achieving 96.8% real-time recognition accuracy (Fig. 2) [4]. Another example is high-speed gas classification using a membrane-type surface-stress sensor. These results indicate that compact, broadband iontronic reservoirs can provide a versatile platform for extracting discriminative spatiotemporal features from raw sensor signals, paving the way toward energy-efficient, material-integrated intelligence at the sensor edge.

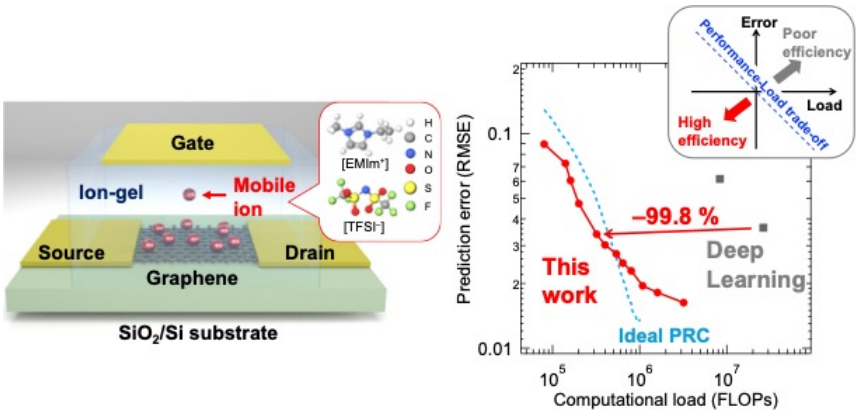


Figure 1. Illustration of ion gel and graphene based ion-gating reservoir (IGR) [2].

Figure 2. Schematic of the real-time spoken-digit recognition framework [4].

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Resistive Random-Access Memory-Based Logic-in-Memory as a Tunable Temporal Encoding Kernel

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Physical reservoir computing (RC) utilizing analog memristors effectively generates non-linear responses to temporal inputs by utilizing the intrinsic dynamic decay characteristics of the devices. However, these conventional analog frameworks suffer from substantial area and energy overheads due to the indispensable peripheral circuits, such as analog- to-digital converters (ADCs). Furthermore, they exhibit prolonged latencies while waiting for state relaxation and suffer from degraded computing reliability owing to inherent device-to-device variation. To overcome these challenges, this study demonstrates a resistive random-access memory-based logic-in-memory as a tunable temporal encoding kernel (RL-TTEK) implemented within a 1-transistor-1-resistive random-access memory (1T–1R) platform to realize non-linear temporal relationships entirely in the digital domain. As illustrated in Fig. 1, the proposed architecture utilizes a fabricated 1T–1R unit device and crossbar array structure alongside a voltage-controlled logic primitive mechanism. Temporal binary input sequences are mapped into the resistive random-access memory array, where memory states are updated through non-linear, logic-in-memory (LIM) operations (such as OR and AND). This deterministic state evolution does not rely on volatile physical relaxation, thereby enhancing the reliability of temporal processing.

To validate the RC capabilities of the RL-TTEK, a system-level hardware architecture was evaluated using the Neuromorphic-MNIST (N-MNIST) spike event-stream dataset (Fig. 2). The kernel hardware, configured as a 784×4 1T–1R array, eliminates ADCs by integrating multiplexers with a high-speed voltage-sense amplifier. Furthermore, by hybridizing complementary OR and AND logic kernels, the reservoir's state separability and classification accuracy are maximized. As a result, the RL-TTEK achieves a high classification accuracy of 92.4% on the N- MNIST task while requiring only ∼18.4 nJ of energy, 24.5 µs of latency, and an ultra-compact area footprint of ∼380 µm^2. These results demonstrate a profound advancement in throughput and hardware efficiency compared to conventional volatile-memristor RC baselines. Ultimately, this work demonstrates a robust, high-speed RC framework that uses digital LIM to implement a tunable temporal-encoding kernel for non-linear projection, providing an efficient hardware paradigm for next- generation edge artificial intelligence.

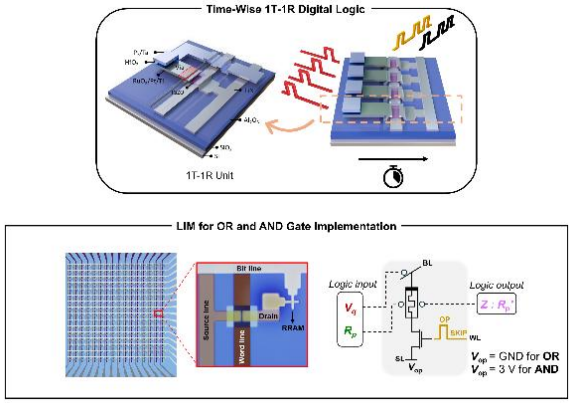


Figure 1. Schematic of the 1T–1R unit device, crossbar array structure, and the voltage- controlled LIM mechanism for non-linear temporal binary input encoding.

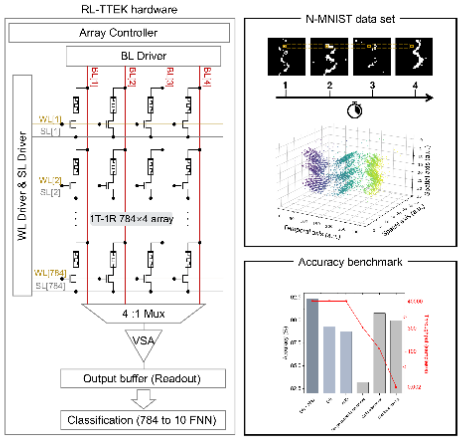


Figure 2. Hardware architecture and RC performance of the RL-TTEK system evaluated on the N-MNIST dataset, utilizing a 784×4 1T– 1R array and a high-speed voltage sense amplifier method to achieve 92.4% classification accuracy.

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Overcoming Dynamic Saturation in Memristor-based Physical Reservoir Computing via Input Spectral Mapping

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Memristive Physical Reservoir Computing (PRC) offers a highly efficient, low-power alternative to traditional recurrent neural networks and computationally expensive sequence modeling architectures for edge computing applications. By leveraging intrinsic nonlinear device dynamics and temporally fading memory, PRC natively implements cumulative information processing. However, physical hardware platforms, particularly memristor-based reservoirs, frequently suffer from a narrow dynamic range compared to standard artificial neurons. Under standard continuous scalar inputs, this constraint leads to severe ”Dynamic Saturation”. Persistently strong signals drive the devices to their conductance limits extremely rapidly—often in fewer than 84 time steps. This rapid saturation suppresses natural decay dynamics, heavily degrades the reservoir’s intrinsic fading memory, and results in redundant, highly correlated features across computing nodes, ultimately neutralizing its computational capacity.

To address this critical hardware bottleneck, we propose Physical Reservoir Computing Input Spectral Mapping (PRISM), a modular input encoding framework designed to limit dense excitation. PRISM regulates excitation sparsity by partitioning the continuous input domain according to the statistical distribution of the time-series data. By employing distribution-aware, unevenly-spaced partition boundaries and a locally continuous sparse encoding scheme, PRISM ensures that each partition contains an approximately equal number of input samples. Furthermore, PRISM utilizes soft linear interpolation between neighboring partitions to maintain information fidelity and sensitivity to fine-scale temporal structures. This distributes the input energy evenly across the physical reservoir nodes (PRNs), preventing any single device from being disproportionately activated and providing the necessary relaxation time to preserve intrinsic temporal memory.

We empirically evaluated the PRISM algorithm on an ensemble of WOx-based memristor devices through both extensive hardware simulations and actual physical device measurements, focusing on canonical chaotic time-series benchmarks. To ensure robustness, our simulations incorporated realistic device constraints and stochastic perturbations emulating fabrication variability, such as per-device decay variation, which were corroborated by experimental measurement outputs from the physical memristor-based RC system. Hardware-level evaluations demonstrate that PRISM fundamentally mitigates the rapid dynamic saturation observed in scalar approaches. Frequency domain analysis reveals that PRISM effectively prevents energy concentration at specific frequencies, preserving temporal diversity and fine-grained details. By distributing the signal amplitude into sparse spectral channels, the devices maintain rich, unsaturated states. While short-term prediction accuracy remains comparable to conventional methods, PRISM’s true advantage emerges in long-term autonomous forecasting and under resource-constrained conditions. Notably, actual experimental measurements of autonomous prediction reveal that while the prediction error (RMSE) of the scalar approach diverges continuously without bounding, PRISM’s RMSE successfully saturates and stabilizes at approximately 30∼33%, demonstrating robust error convergence. Furthermore, in hardware simulations, PRISM substantially reduces the 300-step-ahead prediction error by up to 33% (from 0.3992 to 0.2683) in the Mackey-Glass system. Consistent long-term stability improvements were also observed across the Lorenz and Rössler systems. These results underscore that hardware-aware sparse input mapping is essential for maximizing the representational power and computational reliability of memristive PRC architectures.

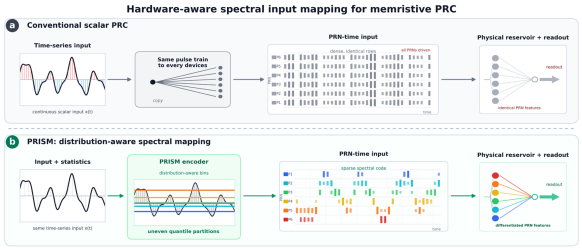


Figure 1. Comparison of (a) conventional scalar-based PRC, which broadcasts dense, identical inputs to all physical reservoir nodes (PRNs), and (b) PRISM, which employs a sparse, differentiated input scheme across the PRN network

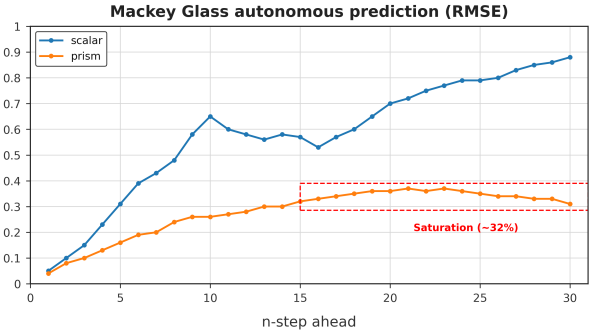


Figure 2. Comparison of long-term autonomous prediction performance for the Mackey-Glass system. While the scalar approach shows continuous error growth, the PRISM method demonstrates better performance, with the error saturating at approximately 30–33%.

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Spatiotemporal Sequence Identification with Percolating Networks of Nanoparticles

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Percolating networks of nanoparticles (PNNs) are brain-like systems that exhibit spatiotemporal correlations and criticality [1], properties that mirror the spatiotemporal signaling employed by the brain [2]. Reservoir computing (RC) is a computing paradigm that exploits the dynamics of the network to project inputs into a high-dimensional state space, from which a simple linear readout extracts the desired output. PNNs have demonstrated strong performance across a variety of temporal tasks [3], yet their capacity to process more complex spatiotemporal signals remains largely unexplored.

Here we build on recent work that has shown that the addition of molecular memristors within PNNs enables learning and forgetting behaviour [4] and enhances performance in RC tasks [5]. We exploit these memristive dynamics to establish PNNs as an effective neuromorphic platform for identifying spatiotemporal sequences.

The sequences of interest are encoded as voltage pulses that are applied to different inputs to the network at different times, as illustrated in Fig. 1. A single linear readout layer is trained, i.e. the Moore-Penrose pseudo-inverse is used to calculate weights for the classification. This allows us to classify up to 40 distinct nine-pulse spatiotemporal sequences with 100% accuracy (Fig. 2 presents a 10 sequence classifciation) The accuracy remains ∼77.3% for 5% input noise. However, the ultimate limits in terms of number of sequences and noise tolerance are under investigation. This approach requires no backpropagation or weight updates within the network and relies on only simple encoding for the inputs. These results position parameter-tuned PNN reservoirs as a practical and scalable platform for order-sensitive temporal pattern recognition in neuromorphic hardware.

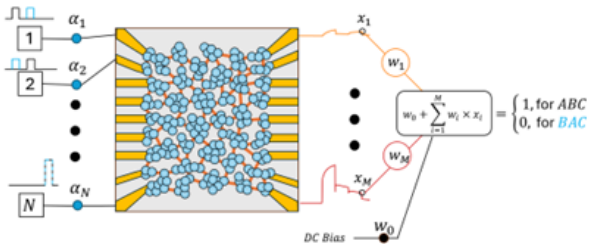


Figure 1. Schematic of the system. Normalized inputs are spatially and temporally input into the network; the output currents are measured at the end of the sequence

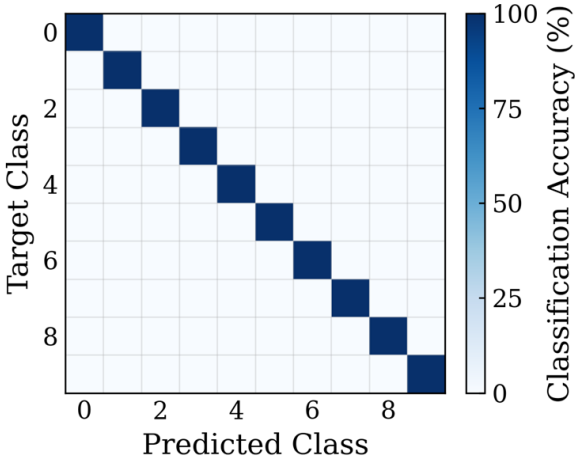


Figure 2. Confusion matrix for spatiotemporal sequence classification. The matrix is an average of 15 independent trials. For each trial, classification outputs are binarised using a winner-takes-all scheme, and the resulting matrices were averaged to yield the proportion of trials in which each sequence (true class) was assigned to each predicted class.

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An Analog Pulse Amplitude-to-Width Encoding Circuit Using Single-Transistor-Latch Oscillator for Reservoir Computing

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Conventional CMOS-based pulse width modulation (PWM) circuits suffer from large area and high energy consumption, severely limiting their integration into compact edge-computing nodes. To overcome these limitations, this work proposes a compact and low-power PWM circuit (Fig. 1). The proposed circuit exploits the unique Single-Transistor Latch (STL) phenomenon inherent in a Silicon-on-Insulator Floating-Body (SOI-FB) MOSFET. By utilizing the nonlinear dynamics of this single-transistor (1T) neuron device, a highly efficient, self-sustained STL oscillator is established without the need for complex multi- transistor configurations.

While functioning as a highly efficient PWM circuit, the proposed circuit is uniquely capable of operating as a real-time analog pulse amplitude-to-width encoder by dynamically interfacing with external variables. Unlike conventional CMOS approaches that require power-hungry, area-intensive data converters (e.g., ADCs or DACs) to process analog inputs, the proposed architecture achieves direct signal transformation without them. As shown in Fig. 1, the oscillating output voltage (V_{source}) from the 1T neuron is fed into a comparator on a custom evaluation board, where it is continuously compared with incoming external analog pulse signals (V_{ref}), such as sensor inputs. The comparator dynamically encodes the multi-level voltage amplitudes of these sensor signals into pulse lengths without any intermediate data conversion stages. The experimental transient characteristics under sequential V_{ref} values as illustrated in Fig. 1, confirm stable, reproducible, and highly nonlinear multilevel encoding capabilities.

To evaluate the hardware feasibility for reservoir computing, the encoded pulse streams featuring variable pulse widths but identical amplitudes were applied to a physical reservoir device fabricated with a Pt/HfO_2/TiN stack. Experimental results of the reservoir device responses in Fig. 2 demonstrate distinct, nonlinear output states corresponding to the modulated pulse widths, confirming its capacity for temporal feature transformation. Crucially, because the original oscillating pulses generated by the 1T neuron inherently exhibit complex nonlinear dynamics, their interaction with the memristive device adds exceptional richness to the system's overall nonlinearity. By modulating information via pulse width rather than amplitude, it suppresses device-level electrical stress to manageable levels while providing superior noise immunity. Consequently, the proposed STL-based circuit provides a highly scalable, area-efficient, and stress-aware interface solution for robust, high-performance hardware reservoir computing.

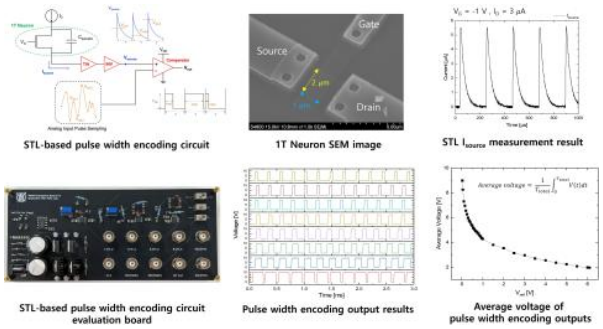


Figure 1. STL-based pulse width encoding circuit & measurement setup & results

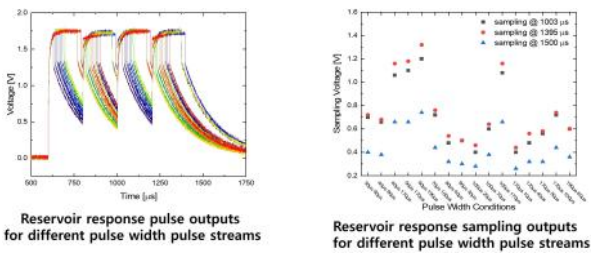


Figure 2. Pulse width-based reservoir computing results

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Multiterminal characterization of spatio-temporal dynamics in self-organizing nanowire networks

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Self-organizing nanowire networks have recently been employed as physical substrates for unconventional computing paradigms, such as reservoir computing, owing to their unique brain-like properties, including spatio-temporal dynamics, emergent behavior, nonlinearity, and heterosynaptic plasticity [1].

Within this framework, the multi-terminal electrical characterization of these complex local spatio-temporal dynamics is crucial for maximizing computational performance.

This work focuses on the role of the areal mass density (AMD) in nanowire networks, demonstrating that it not only affects the global connectivity and conductance of the network, but also tunes information persistence and synchronization over time [2].

Furthermore, the extension of the concepts of memristance and transmemristance from two-terminal systems to generic multi-terminal devices is presented [3].

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Talks

Noise

Understanding and Controlling Read Noise in VCM-based RRAM

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Filamentary valence change mechanism (VCM)-based resistive random-access memories (RRAMs) have emerged as promising candidates for artificial synapses in neuromorphic computing due to their ability to encode synaptic weights through multiple conductance states. However, the intrinsic stochasticity associated with defects migration within the switching layer strongly impacts the short-term stability of programmed states, posing a major challenge to achieving stable and reliable multilevel operation [1,2]. Understanding and controlling these instabilities is therefore essential for the deployment of VCM-based RRAM in emerging computing applications.

Here, we investigate the short-term stability of VCM-based memories across both industrial-scale and laboratory-scale devices. Mbit-scale VCM arrays integrated into 28 nm CMOS reveal characteristic read noise arising from the dynamic equilibrium of oxygen vacancy diffusion, causing short-term instability at the individual device level while remaining statistically stable across large device populations [3].

Complementary laboratory-scale studies demonstrate that the amplitude and spectral characteristics of the read noise strongly depend on the underlying conduction mechanism of the switching oxide. Analysis of different switching oxides reveals that materials with shallow defect states exhibit higher signal-to-noise ratios, whereas oxides with deep defect states show pronounced ionic noise driven by vacancies relocation [4]. These findings establish a clear correlation between conduction mechanism and read-noise characteristics, enabling the tuning of the device performance through material design. Furthermore, process parameters and read conditions are identified as key levers for controlling short-term variability, providing practical routes for device optimization and improved operation [5].

Building on these findings, a denoising strategy is investigated to mitigate stochastic fluctuations in the programmed states, supporting reliable multilevel programming. Unlike previously reported approaches based on repeated write-read cycles and continuous noise monitoring [6], the proposed method employs fixed electrical stress pulses applied immediately after programming, reducing read noise with minimal operational overhead. Experimental validation on VCM-based 1T1R (one-transistor–one-memristor) devices demonstrates a significant reduction in read-current fluctuations and effective stabilization of the programmed high resistance state (HRS) [7]. HRS stabilization is of primary importance for enabling reliable multilevel operation, as it is the state most strongly affected by read noise. Similar denoising strategies are currently being optimized for the low-resistance state (LRS) and intermediate conductance states, aiming to further reduce read noise and increase the number of reliable programmed conductance levels.

Beyond representing a source of variability, the intrinsic stochasticity of VCM devices can also be harnessed as a functional resource by directly exploiting read noise as a source of randomness. In particular, it has been shown that VCM devices with deep defect states provide high-quality entropy sources for true random number generation, enabling single-step random bit extraction while successfully passing NIST randomness tests [8].

Together, these results establish a comprehensive framework for understanding and controlling short-term instability in VCM-based RRAM technologies, enabling application-specific optimization in which intrinsic stochasticity can either be deliberately exploited, or mitigated to improve reliable multilevel programming.

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Low-Frequency Noise Uncovers Distinct Filament Dynamics in La-Doped and Undoped HfO_2-Based RRAM

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Resistive random-access memory (RRAM) devices are promising candidates for neuromorphic computing due to their scalability, low power operation, and capability to emulate biological synapses through gradual conductance modulation and history-dependent dynamics. As low-frequency noise (LFN) directly influences readout accuracy and increases system stochasticity, understanding and tailoring noise characteristics is essential for reliable neuromorphic implementations.

In this work, a systematic analysis of noise behavior is performed under varying reset voltages and DC cycling conditions for lanthanum-doped (La:HfO_2)- and undoped HfO_2-based RRAM devices. The results reveal fundamentally distinct filament dynamics and noise characteristics between two devices. In particular, La doping leads to enhanced current uniformity and a significant narrowing of the read current distribution across multiple resistance states, indicating improved filament stability and readout reliability. Combined with the inherent gradual switching behavior of La:HfO_2-based devices [1], it emphasizes its importance as a promising candidate for multi-level to analogue switching.

Comparing the HRS, the incomplete rupture of the filament in La:HfO_2, and the complete rupture in HfO_2 under varying reset voltages affect the noise behaviour. While both show a two-stage scaling of the normalized noise magnitude with device resistance, the HfO_2 system first increases, and, after a corner point at ∼6 MOhm, decreases, as a result of trap-redistribution, whereas the La:HfO_2saturates above ∼5 kOhm. Complemented by the investigation of the LRS, a resistance–noise scaling rule spanning a wide resistance range is developed (Fig. 1), offering insights into noise tailoring strategies for HfO_2-based system.

Furthermore, noise evolution during DC cycling also exhibit different trends. Noise suppression with cycling is observed in both the HRS and LRS of undoped HfO_2 devices and is attributed to the continuous incorporation of traps into the conductive filament [2], as evidenced by a decrease in resistance. Comparatively, no clear trend is detected in the La:HfO_2 devices. In the HRS, a stable saturated noise magnitude over hundreds of cycles indicates enhanced filament stability and reduced variability, while the fluctuating noise level in the LRS could be attributed to the presence of La atoms, which act as preferential accumulation sites for oxygen vacancies, thereby modulating the effective trap density in the vicinity of the filament over repeated cycling.

This study demonstrates the critical role of defect engineering in controlling noise characteristics of RRAM devices and provides a viable approach for noise tailoring through resistance tuning and DC cycling in HfO_2-based RRAM devices.

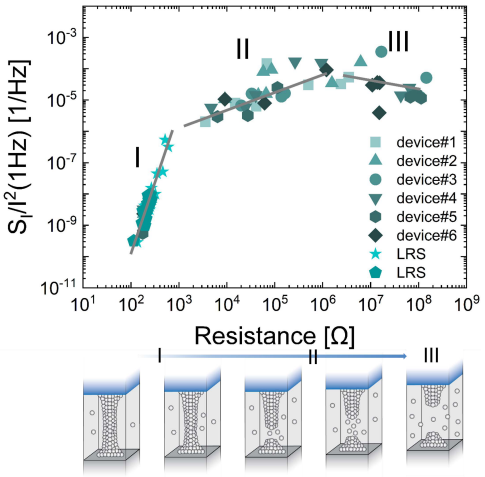


Figure 1. Three-stage resistance scaling of noise magnitude over a wide resistance range with the schematic illustration in below. In stage I, a higher scaling factor is associated with the lateral scaling filament; in stage II, the noise amplitude continuously increases with resistance as a result of the increased gap length; in stage III, the trap re-distribution leads to a reduction of trap density around the filament region, resulting in a reduced noise level.

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Full-cycle noise measurements in memristive systems: uncovering and reducing the stochasticity that limits device performance

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Programming accuracy, reproducible operation, and high endurance are key technological requirements for memristive devices utilized in neural network applications. In memristive artificial synapses, driftless data retention and fine resolution of programmable conductance weights are critical for device operation, whereas in volatile neuron-like devices the variability of the switching threshold voltage becomes a key limiting factor. However, inherent fluctuations in the ultra-small active volume of nanoscale devices impose fundamental limits on the above performance metrics. In order to understand and push these limits, a comprehensive noise benchmarking and noise reduction protocol is introduced [1].

We demonstrate the noise map of steady-state fluctuations by comparing the relative readout noise levels of different filamentary and phase-change-type memristive devices and their scaling with the programmable device conductance [2]. Furthermore, our approach goes beyond the measurement of steady-state readout noise levels and tracks the voltage-dependent noise characteristics all along the resistive switching I(V) curves. We investigate the cycle-to-cycle variation of fluctuations in our memristive devices. This analysis highlights a broad, order-of-magnitude variability of the possible noise levels behind seemingly reproducible switching cycles in Ta2O5 filamentary memristors [1]. Our nonlinear noise spectroscopy measurements identify a subthreshold voltage region with voltage-boosted fluctuations. This voltage range enables the reconfiguration of the fluctuators without resistive switching, yielding a highly denoised state within a few subthreshold cycles.

Finally, extending the nonlinear noise spectroscopy approach to volatile VO2 memristive systems, we demonstrate that the noise enhancement observed in the vicinity of the switching threshold is quantitatively consistent with the cycle-to-cycle threshold voltage variability [3], which limits the reproducibility of artificial neuron operation.

Our results demonstrate a direct link between measured fluctuations and the stochasticity of device dynamics, highlighting the potential of full-cycle nonlinear noise spectroscopy as a framework for identifying performance-limiting factors in different types of memristive devices beyond traditional characterization methods.

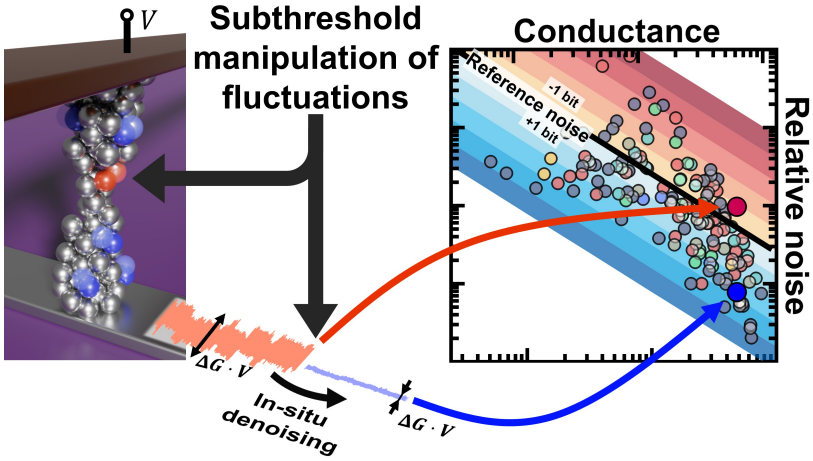


Figure 1. Demonstration of denoising by sub-threshold voltage cycling. Driving the device slightly out of its steady state triggers the reconfiguration of the fluctuators, enabling travel across the noise map from a higher-noise state to a lower-noise state.

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Temperature dependent characterization of HfO2 memristive devices and their noise analysis

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The memristive devices in this study have shown high endurance (∼10000 cycles) and retention of low resistive state (LRS) (90500 seconds). Notably, LRS values of devices with different active layer thickness or device diameter have been recorded near quantum conductance states (0.5G0, 1G0, 2G0 where (1/G0≈ 12.9 kΩ). The robust characteristics of these devices allows comparison between devices of different active layer thicknesses and diameters and has also encouraged investigating SET probability and temperature dependent measurements. Temperature-dependent characterization is critical for elucidating the underlying transport mechanisms across different resistance states and assessing the nature of conduction in memristive devices {1]. A cryo-probe station was used for the temperature dependent measurements, which enables tracking the change in resistance at cryogenic temperatures without the mechanical and electrical stress that wire bonding causes, allowing for more repeatable measurements.

Noise performance of memristive devices remain largely limited even though noise performance of electronic circuits is a foundational benchmark to evaluate reliability [2]. Random Telegraph Noise (RTN) is a stochastic switching phenomenon observed in solid state electronic devices, occurring due to trap and release of charge carriers in semiconductors [3]. Characterizing noise across different resistance states (HRS, LRS, nG0) and temperatures allows for the decoupling of thermal noise and RTN, with low-temperature measurements enabling the isolation of pure RTN.

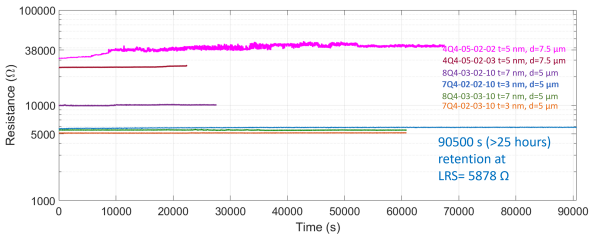


Figure 1. Retention measurements of different device geometries at LRS

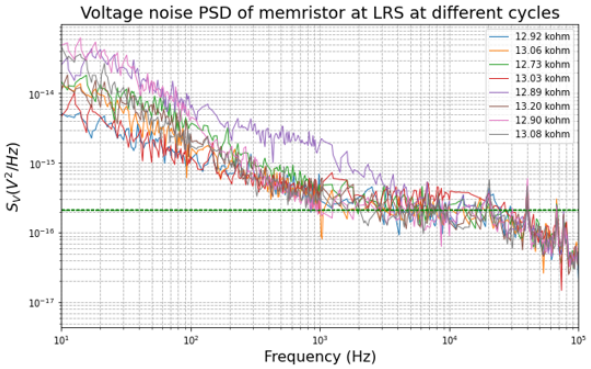


Figure 2. Voltage noise PSD at LRS in room temperature

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AFM-based local fluctuation spectroscopy of memristive systems

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The inherent fluctuations in the active volume of memristive devices fundamentally determine their operational characteristics, for instance, the device noise imposes severe constraints on the weight resolution in hardware neural network applications [1,2]. On the other hand, some probabilistic computing approaches require intentionally enhanced, and tunable noise levels [3,4]. Furthermore, the understanding of the noise properties also aids the understanding of the fluctuation sources and the optimizations of device fabrication [5].

Here, we present a comprehensive local probe noise measurement methodology that goes beyond the characterization of steady-state readout noise and tracks the voltage-dependent fluctuation properties. While such measurements are typically performed on complete devices [2], performing fluctuation spectroscopy with nanoscale spatial resolution would provide valuable insight into the spatial distribution of fluctuation sources and their relation to the active switching regions.

To address this challenge, we implement the methodology in a conductive atomic force microscopy (C-AFM) platform, enabling local fluctuation spectroscopy with nanometer-scale spatial resolution. In this work, a Semilab tabletop AFM system was combined with an Emerson NI FPGA-based measurement system to enable spatially resolved noise measurements on planar vanadium dioxide (VO_2) memristive samples. The AFM tip is first used as a force sensor to map the nanoscale topography of the sample and subsequently as a local top electrode for targeted noise measurements in regions of interest. These results demonstrate the feasibility of local fluctuation spectroscopy and establish the suitability of the combined setup for spatially resolved noise characterization of memristive materials and devices.

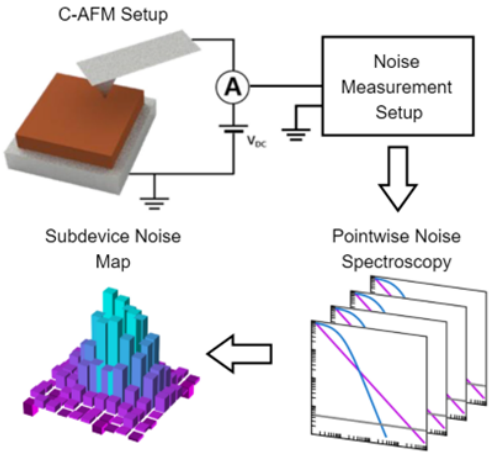


Figure 1. Schematic representation of spatially-resolved noise characterization via local probing.

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Talks

Uncommon Systems

Programmable memristors with two-dimensional nanofluidic channels

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Nanofluidic memristors, obtained by confining aqueous salt electrolyte within nanoscale channels, offer low energy consumption and the ability to mimic biological learning. Theoretically, four different types of memristors are possible, differentiated by their hysteresis loop direction. Here, we show that by varying electrolyte composition, pH, applied voltage frequency, channel material and height, all four hysteresis-loop types can emerge in nanofluidic systems. We show that our channels display both volatile and non-volatile memory, including short-term depression akin to synapses, with signal recovery over time.

Furthermore, we demonstrate nanofluidic ionic memory from highly-ordered angstrom-scale pores in covalent-organic framework membranes. Ionic materials can store electrical history through ion redistribution, interfacial polarization and charge transport, yet these processes are often treated as separate resistive and capacitive contributions. Here we show that an ultrathin covalent organic framework membrane with ordered nanopores couples these degrees of freedom within a single confined ionic material. The ionic environment around these membranes with pores can support physical variables for realizing higher-order learning.

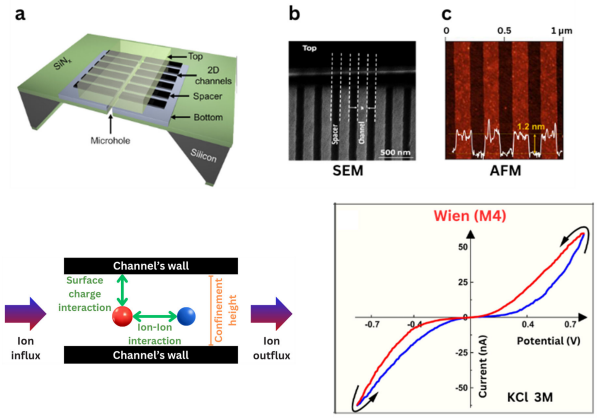


Figure 1. Schematic of angstrom-scale channel device, with scanning electron microscopy and atomic force microscopy of the channels shown alongside. Below, the memory mechanism arising from the ion-ion and ion-wall interactions is shown schematically, along with a typical current-voltage hysteresis curve.

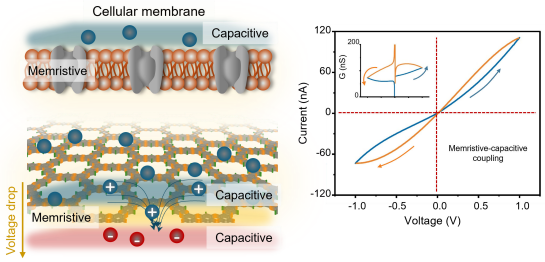


Figure 2. COF membranes with ordered pores analogous to natural lipid bilayer membranes with nanochannels, Current-voltage characteristics showing pinched hysterisis loop from COF membranes.

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From Powder to Device: High Entropy Oxide for Resistive Switching Applications

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High entropy oxides (HEOs) are emerging as promising materials for resistive switching applications due to their unique structural and electrical properties. Comprising multiple principal metal cations in a single-phase solid solution, HEOs exhibit high configurational entropy that enhances thermal stability, tunable electronic properties, and defect engineering—key factors for resistive switching devices. [1]

Resistive random-access memory (RRAM) relies on reversible resistance changes under an electric field, with HEOs offering advantages such as improved endurance, scalability, and lower power consumption. [2] The synergistic interactions among cations create a defective lattice structure that affects oxygen vacancy migration, crucial for resistive switching. Due to CMOS compatibility and tunable material properties as a function of dopants, studying binary systems such as NbTaOx or ZrHfOx offers a promising pathway for energy-efficient, and cost-effective HEO-based non-volatile memory solutions with selected elements, providing a beneficial, synergestic cocktail effect. Nb is known to act as an amorphizing agent that increases thermal stability of doped Ta2O5 thin films. [3] Thanks to the high solubility limit (50 Mol%) of Nb2O5 in β-Ta2O5 in accordance with the Hume-Rothery rules, NbTaOx solid solution systems offer a wide range for in-depth studies.

In this study, we demonstrate the resistive switching behavior of NbTaOx thin films, prepared from in-house synthesized ceramic targets using a solig-state reaction method. For this purpose, powder synthesis involved homogenization and comminution via mechanical milling of equimolar mixtures of Nb2O5 & Ta2O5 before and after calcination at 1000°C. Fabrication of targets was carried out by Spark-Plasma Sintering at 1000°C applying a uniaxial pressure of ∼30 MPa. The thin film was deposited via RF-sputtering, and its structural and compositional properties were analyzed using X-ray photoelectron spectroscopy (XPS) and X-ray diffraction (XRD). Pt/Oxide/Ta/Pt RRAM devices with a 2x2 μm^2 cell size were fabricated through photolithography and dry etching processes. Electrical characterization using a Keithley 4200 SCS parameter analyzer revelead that NbTaOx-based devices show significantly reduced variability in key characteristics such as the high and low resistive state (HRS & LRS), as well as the switching voltages (See Fig. 1). The NbTaOx devices demonstrated a fast SET time of 10 ns, endurance exceeding 10^8 switching cycles, and a retention of well over 10 years at 85°C (See Fig. 2). With their promising performance, NbTaOx materials offer potential for further research into high-entropy oxides as candidates for next-generation RRAM. Given the promising results obtained by using NbTaOx, we further research focusing on high-entropy oxides in pursuit of a material for RRAM that can satisfy the requirements of modern memory devices.

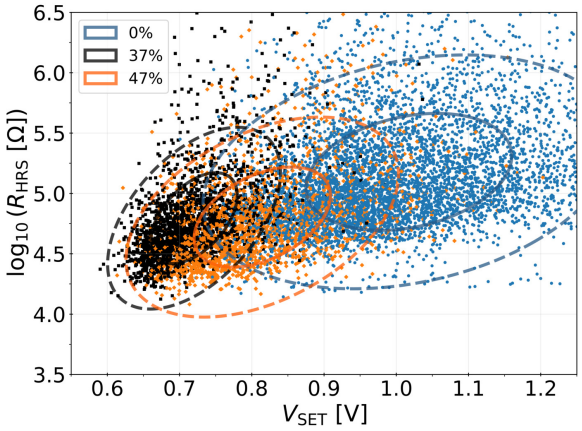


Figure 1. SET voltage & HRS correlation plot illustrating the improved variability for NbTaOx-based devices with 37% and 47% Nb compared to 0% Nb (TaOx).

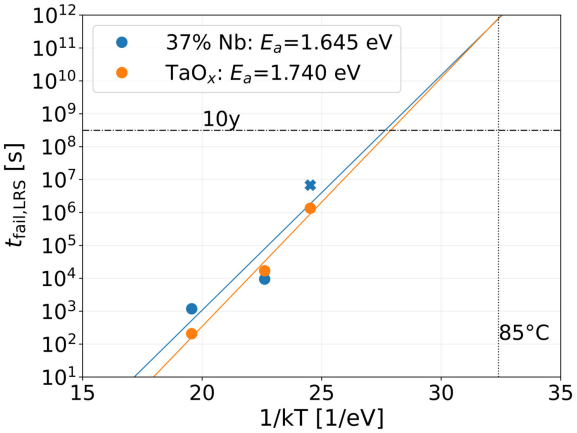


Figure 2. LRS retention arrhenius plot illustrating the excellent retention of our TaOx and NbTaOx-based devices. Ea denotes the activation energy.

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Temperature Induced Synaptic Fatigue in BiFeO3-Based Electronic Synapses

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Neuromorphic computing devices, inspired by the signal processing and memory functions of biological neural networks, are highly influenced by temperature-dependent charge transport mechanisms. In the present work, $BiFeO_3$ (BFO) thin films were fabricated by Pulsed Laser Deposition and incorporated into Au/BFO/FTO structures. The impact of temperature on both the ferroelectric and neuromorphic properties of these devices was systematically studied between 40 and 120 °C.

At lower temperatures, the devices exhibited stable synaptic responses and effective pattern recognition capability. However, a gradual deterioration in neuromorphic performance was observed with increasing temperature, becoming particularly pronounced above 100 °C. To elucidate the origin of this behavior, temperature-dependent electrical transport was investigated through current–voltage analysis using Arrhenius, space-charge-limited conduction (SCLC), Poole–Frenkel, and Schottky emission models. The results indicate a thermally activated conduction mechanism characterized by an activation energy of approximately 0.79 eV, suggesting the involvement of oxygen-vacancy-mediated transport.

Furthermore, increasing temperature drives a transition from trap-dominated SCLC to a conduction regime approaching ohmic behaviour, attributed to trap activation and enhanced carrier mobility. Simultaneously, ferroelectric characterization reveals a progressive reduction in remnant polarization (Pr) and hysteresis loop area, reflecting weakened ferroelectric order. The combined influence of modified charge transport dynamics and diminished ferroelectric polarization is found to be responsible for the loss of synaptic performance at elevated temperatures.

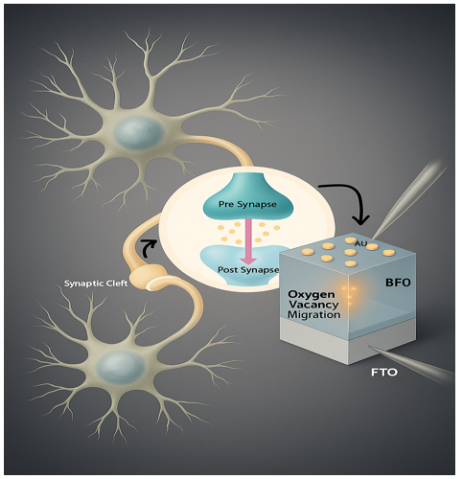


Figure 1. Schematic of the Au/BFO/FTO neuromorphic device, where oxygen-vacancy migration in the BFO layer enables synaptic behaviour analogous to a biological synapse

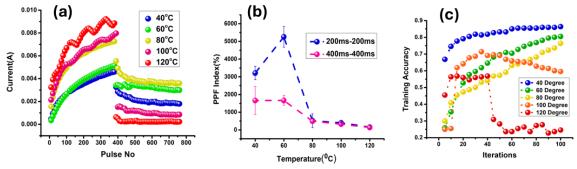


Figure 2. Effect of temperature on (a) synaptic plasticity, (b) PPF response, and (c) pattern recognition accuracy of the Au/BFO/FTO neuromorphic device.

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Inkjet-Printed Hexagonal Boron Nitride Memristors: Current-Driven Characterization and Record Endurance at Low Switching Currents

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The exponential growth in energy consumption driven by the development of artificial intelligence systems poses a significant sustainability challenge [1]. Memristors have emerged as key electronic devices for enabling low-power neuromorphic computing. In particular, inkjet-printed memristors stand out due to their additive manufacturing process, lower fabrication costs, and compatibility with flexible substrates, facilitating the development of low-cost, flexible, and biocompatible applications [2,3]. However, further improvements in device performance, including endurance and low switching currents, are still required to meet the demands for effective implementation in neuromorphic systems.

In this work, we present an inkjet-printed hexagonal boron nitride (h-BN) memristor that exhibits both non-volatile and volatile resistive switching (RS) characteristics. For current compliances ranging from 10 μA to 1 mA, the devices demonstrate non-volatile RS with resistance ratios of approximately 10^5 under ramped voltage sweeps. In contrast, operation at significantly lower current compliances (from 1 nA to 100 nA) induces volatile RS behavior, resulting in a resistance ratio up to 10^2 for the highest compliance within this range. Notably, both switching regimes operate at relatively low currents and low voltages.

A further key contribution of this work is the comparison between current-driven and voltage-driven memristor operation. While current-driven characterization remains largely unexplored, achieving precise control under this operating mode is essential for the development of current-driven neuromorphic computing systems. To investigate this aspect, ramped current sweeps were performed in both switching regimes. The resulting current-voltage curves exhibited pronounced hysteresis while displaying switching signatures markedly different from those observed under voltage-driven operation. These findings demonstrate that current-driven characterization provides complementary insights into memristive behaviour and represents a promising yet underexplored approach for the analysis and control of memristive devices.

Under the current-driven approach, pulsed endurance tests were conducted. Record endurance values for inkjet-printed memristors were achieved in both regimes, reaching 60,000 cycles in the non-volatile regime and 2 million cycles in the volatile regime, with minimal state overlap. These results significantly exceed the endurance typically reported for inkjet-printed memristors, which rarely surpass 1,000 cycles [4-6]. These results demonstrate exceptional endurance, reliability, and low-current operation, while paving the way for current-driven neuromorphic computing and establishing hexagonal boron nitride as a promising material for next-generation inkjet-printed memristive devices.

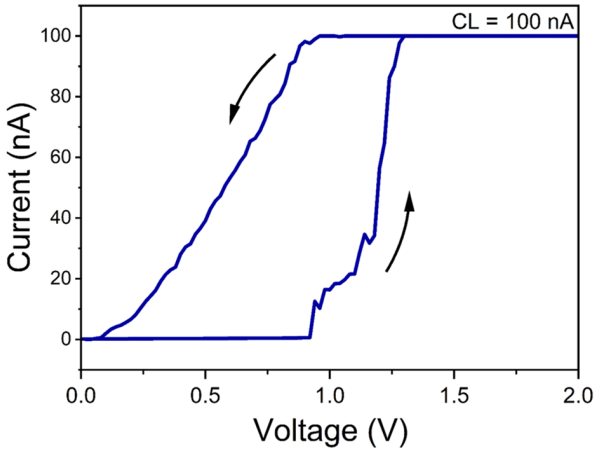


Figure 1. Current-voltage (I-V) curve of an inkjet-printed Ag/h-BN/Au memristor obtained during a ramped voltage sweep with a 100 nA current limitation, demonstrating volatile resistive switching.

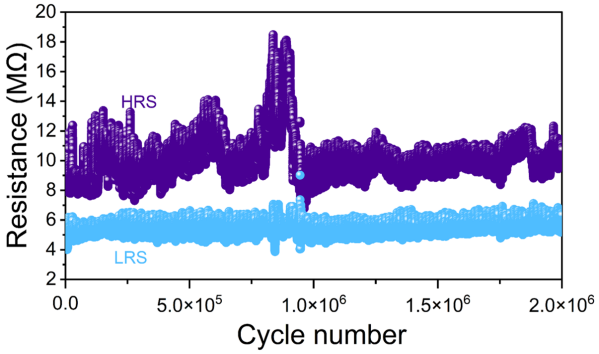


Figure 2. Endurance of the inkjet-printed Ag/h-BN/Au memristor in the volatile regime, demonstrating stable switching over 2 million cycles with minimal state overlap under pulsed current excitation.

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Programming Noise Mitigation of Synaptic Weights Through Adaptive Quantization in Spintronic Resistive Devices

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Programming variability limits the precision of resistive-memory synapses and consequently degrades the performance of analogue in-memory computing systems. Here, we introduce a programming-noise mitigation strategy that combines resistive switching and magnetoconductance in spintronic resistive devices. The synaptic weight is encoded by the total conductance of three La0.7Sr0.3MnO3/tris(8-hydroxyquinolinate)gallium/AlOx/Co molecular spin valves connected in parallel[1], [2]. Resistive switching first programs the conductance close to a target value, while the magnetic configurations of the constituent devices provide eight additional, approximately equally spaced, conductance states for fine weight adjustment. This is achieved by ensuring that the magnetoconductance ΔG_1 of each of the crosspoints follows the law:

$$\Delta G_1 = 2 \times \Delta G_2 = 4 \times \Delta G_3 = \cdots = 2^{N-1} \times \Delta G_N \quad (1)$$

By setting the magnetoconductance contributions in this binary proportions, the accessible magnetic states form an adaptive quantization ladder whose span is controlled by the programmed resistive state. We experimentally demonstrate the required conductance relationships and model the coupled resistive and magnetic response under cycle-to-cycle variability. The resulting synapse is evaluated in a deep-Q-learning network solving the cart- pole balancing task. Compared with a conventional resistive implementation using the same number of crosspoints, adaptive magnetic quantization substantially improves robustness to programming noise. At 5% conductance-noise standard deviation, the average reward increases from 39 ± 5 to 130 ± 7. These results establish resistive–magnetic adaptive quantization as a general route toward more accurate and noise-tolerant neuromorphic hardware.

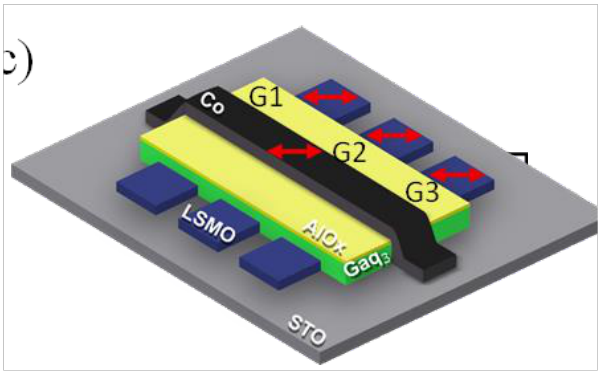


Figure 1. Fig. 1: Schematic representation of the multi-weight synapse, made from LSMO/Gaq3/AlOx/Co stacks. Thanks to its spintronic properties, the conductance G_n of each crosspoint depends on the relative orientation of the ferromagnetic electrodes (parallel or antiparallel), indicated the red arrows. In this work we concentrate on three-crosspoints devices, although the concept can be generalized to N, for a total of 2^N possible magnetic states. Fig. 2: Experimental realization of the adaptive quantization protocol in an artificial synapse made from three physical crosspoints in an experimental multi-weight synapse being set in the quantized state described in equation (1). Each curve reports the conductance of each crosspoint measured as function of the magnetic field. The empty symbols are for data measured as the magnetic field went from +300 mT to −300 mT whole the full ones are representing data taken with the field going from -300 mT to + 300 mT. When the applied magnetic field B was of a sufficiently high intensity (i.e. |B|>120 mT, the magnetization of the electrodes was parallel (P) in all crosspoints and the conductance was G_P ($G_{1,P}$ ≅31 µS, $G_{2,P}$ ≅27 µS, $G_{3,P}$ ≅24 µS). When the magnetic field was lowered and changed sign, the coercive field of the LSMO electrode was reached and the magnetization was in the antiparallel (AP) state G_{AP} ($G_{1,AP}$ ≅33 µS, $G_{2,AP}$ ≅28 µS, $G_{3,AP}$ ≅24.5 µS). $\Delta G_n$is defined as $\Delta G_n = G_{n,AP} - G_{n,P}$. As the field was increased further and reached |B|>120 mT, the magnetization configuration flipped back to parallel. The blue curve is the most significant bit, the black one is the list significant bit and the red one is intermediate one: ΔG_3 ≅2.09 µS≅2 × ΔG_2 ≅0.96 µS= 2 × ΔG_1 ≅0.48 µS.

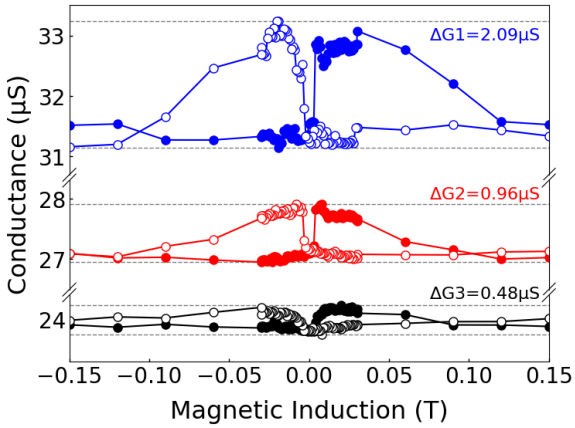


Figure 2.

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Flexible LIG CuO/ZnO pn Nanoheterostructure for Efficient CO Detection at Room Temperature

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ZnOnanorods (NRs) have been dropcast onto Laser Induced Graphene (LIG). The LIG substrates were treated by oxygen plasma to modify their surface wettability from hydrophobic to hydrophilic, thereby improving the dispersion and interfacial contact of deposited ZnO nanostructures. The effect of plasma treatment on photocatalytic activity was studied by monitoring methylene blue degradation under ultraviolet light for 120 minutes. Compared with untreated LIG/ZnO, the oxygen plasmatreated LIG/ZnO composite exhibited enhanced dye degradation efficiency, attributed to improved dye adsorption and better charge transfer at the LIG–ZnO interface. These findings highlight the role of surface engineering in tuning the photocatalytic performance of LIGbased hybrid systems for wastewater treatment applications. The crystallinity of the deposited ZnO is also proven via XRD analysis. Results show that the photocatalytic performance of the LIGZnO NR increases upon plasma treatment. This work demonstrates a novel, flexible, and easytouse approach by employing oxygen plasmatreated LIG as a hydrophilic substrate for ZnObased photocatalysts. By improving dye adsorption and charge transfer, surface engineering enables the creation of flexible, scalable, and sustainable photoactive materials for advanced environmental remediation.

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Talks

Silicon Oxide / PCMO

CMOS-compatible silicon-oxide memristors: Device characterization, compact modelling, and prospects for in-memory computing

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The growing limitations of conventional embedded Flash memories motivate the exploration of alternative non-volatile memory technologies that can be seamlessly integrated with standard CMOS processes. In this context, silicon-oxide has emerged as an attractive switching material for ReRAM devices, enabling simplified device structures and potentially low-cost fabrication while maintaining compatibility with existing semiconductor manufacturing flows. In this work we present the electrical performance of silicon-oxide 1T1R memristor structures integrated on chip, placing particular emphasis on experimental validation across different measurement levels. Wafer-level characterization is first employed to evaluate device functionality, variability and switching statistics across large device populations, providing a global view of the technology maturity. This analysis is complemented with detailed chip-level electrical measurements of large memristor arrays, where the interaction between the memristive device and the surrounding CMOS circuitry can be directly assessed under realistic operating conditions. In parallel, we address the compact modelling of these devices, which is essential to enable reliable electrical simulations of circuits incorporating memristors. We introduce a modelling framework based on a system of coupled equations that, through different variants, provides a flexible yet accurate behavioural compact model for resistive switching. Finally, to illustrate the relevance of this modelling approach for hybrid CMOS-memristor systems, we briefly discuss its use in the analysis of representative circuit blocks, including the analogue circuitry used to program and sense the memristor state and its potential integration within emerging computing architectures as electronic synapses, for which we show its typical Long-Term-Potentiation and Depression characteristics.

The role of deposition on oxygen exchange at the SiO2/Ta interfaces: a first-principles study

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In recent years, resistive random-access memory (ReRAM) devices have emerged as promising candidates for advanced memory technologies. These devices offer high scalability, high endurance and fast programming speed. Typically, ReRAM consist of a metal oxide sandwiched between two metallic electrodes. Application of a small voltage induces the formation and destruction of a conductive oxygen vacancy filaments in the oxide, enabling switching between high (HRS) and low resistive states (LRS)[1]. As oxygen vacancies are central to the working principle of ReRAM devices, a complete understanding of the formation of such defects at the metal/oxide interface is essential. In this project, we investigate from first-principles the interface between silicon dioxide (SiO_2) and tantalum (Ta). Tantalum has shown excellent ability to promote the formation of oxygen vacancies at the metal/oxide interface by extracting oxygen from the oxide in a process called scavenging [2]. To better understand this exchange, we examine two types of models: full-interface models, consisting of a Ta(110) slab on a SiO_2 surface, and cluster models, consisting of small Tan clusters adsorbed on a SiO_2 substrate. Our goal is to evaluate the transfer of oxygen from SiO_2 to Ta at different stages of film growth. Here, the full-interface models represent a fully formed film, while the cluster models correspond to the initial stages of film growth. For each model, we explore the formation of oxygen vacancies in the SiO_2 substrate and the incorporation of the displaced oxygen into the Ta, either slab or cluster. We investigate this oxygen-transfer process considering its energetic and kinetic aspects. Our findings show that the process is energetically favourable only for the cluster models, suggesting that spontaneous scavenging is likely to initiate during the early stages of film growth. At the same time, however, each model indicates the existence of an energy barrier associated with the breaking of Si-O bonds. With this computational analysis, we aim to shed light on the atomistic processes during a possible scavenging event at the interface between the metal oxide and the metallic electrodes.

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Tracing the origin of switching variability in SiOx:Cu memristive devices through fabrication, data mining and simulations

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In this study, we investigate the origin of switching variability in nominally identical sub-stochiometric SiOx based memristive devices [1] that exhibit different electrical responses. To this end, an integrated workflow combining plasma-assisted fabrication, wafer-level electrical characterization, data-driven classification and device-level simulations is used to establish a consistent picture of switching in these devices. Rather than treating the observed variations as arbitrary deviations, we examine how processing-induced material differences give rise to distinct macroscopic switching responses and microscopic switching mechanisms.

The TiN/SiOx:Cu:SiOx/TiN devices with Cu insertions (Fig. 1a) are fabricated by reactive sputtering. In this process, the deposition environment influences the SiOx composition, Cu incorporation, and local defect landscape. Electrical measurements from over 50,000 devices across 50 wafers are analyzed using data-driven clustering based on self-organizing maps [2]. This analysis reveals distinct switching response types, including capacitive, memristive (interface-type (analog), and filamentary-type (digital)) and resistive switching. The classification as in Fig. 1b indicates that the observed variability adheres to trends across different processing parameters (such as deposition time and plasma power), suggesting that the distinct switching responses are attributable to alterations in the local material configuration.

A key finding is that Cu insertions play a decisive role in enabling and shaping the switching response. STEM and in situ heating experiments show that memristive-like switching is only observed when the Cu insertions agglomerate sufficiently to form Cu nanoparticles. The corresponding I-V characteristics are shown in Fig. 1a. Impedance spectroscopy, area-scaling analysis and curve fitting indicate that charge transport is governed by a heterogeneous Schottky barrier landscape, shaped by Cu morphology, local interface states and ionic defect redistribution. These findings are supported by 1D cloud-in-cell-based device-level simulations, which provide further insight into the microscopic ionic and electronic transport mechanisms [3]. The model as shown in Fig. 2a simulates field-assisted oxygen-vacancy transport through the oxide and describes the device as a back-to-back Schottky contact configuration at the TiN/SiOx interfaces, with Poole-Frenkel conduction in the oxide bulk. By considering four different parameter sets that vary the defect landscape, Cu-morphology-dependent Schottky parameters and oxygen-vacancy transport, the simulations as observed in Fig. 2b reproduce the experimental I-V characteristics identified by the data-driven analysis.

Overall, the study shows that the different switching responses arise from several connected factors, including the plasma process, SiOx stoichiometry, Cu distribution and defect evolution during operation. Bringing together fabrication, material analysis, large-scale electrical data and simulations makes it possible to understand which conditions favour analog-type switching across the wafer. This provides a clearer direction for optimizing the Cu amount and oxide composition toward more uniform and stable memristive devices for neuromorphic hardware. It also suggests that improved process control, scaling and alternative deposition strategies could help reduce the stochastic nature of the switching response.

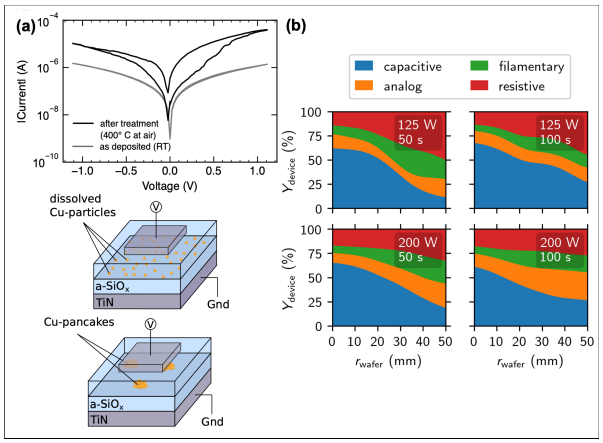


Figure 1. (a) I-V characteristics of of the SiOx:Cu device before and after thermal treatment, with schematics of dispersed Cu insertions and agglomerated Cu. (b) Generalized device yield as a function of radial wafer position with different deposition power and time.

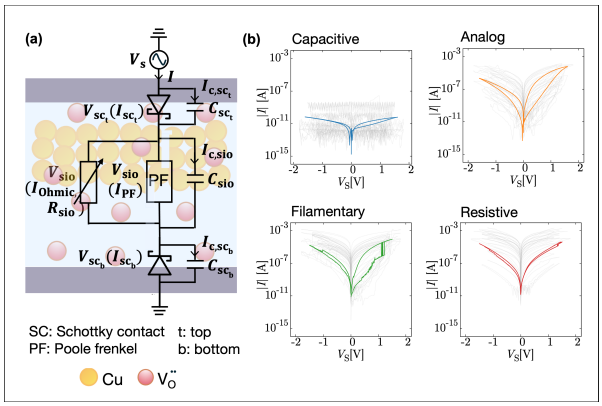


Figure 2. (a) Equivalent circuit used in the 1D device-level simulation model. (b) Simulated I-V characteristics of the four clusters identified in Fig. 1(b), with gray curves showing the corresponding experimental I-V curves.

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Detection and Statistical Analysis of Switching Behavior Transitions in SiOx-Based ReRAM

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Resistance switching devices offer promising prospects for embedded memory and neuromorphic computing. The complex and convoluted physical processes that provide such opportunities are, on the other hand, hard to control and pose device engineering and operation optimization challenges. One of the main obstacles is variability. In addition to expected device-to-device and cycle-to-cycle variability there are transitions in the device response as it deteriorates. Learning how to minimize degradation and ensure repeatability is crucial for most applications. In this work SiOx redox-based random access memory (ReRAM) cells were tested to explore atypical filamentary switching events and connect them to transitions in electrical metrics through statistical analysis. The measured dataset includes data from pulsed amplitude sweeps with varied timings and different resistance targets to investigate how the switching behavior can be changed by device programming conditions. Using the collected data, we developed a method based on quantized conductance theory to qualitatively categorize the switching curves. The classification labels were then used to unveiled distinct switching patterns, changes in measured metrics, and transitions in operational modes. The results help narrow down possible underlying physical processes and guide further ReRAM stack development.

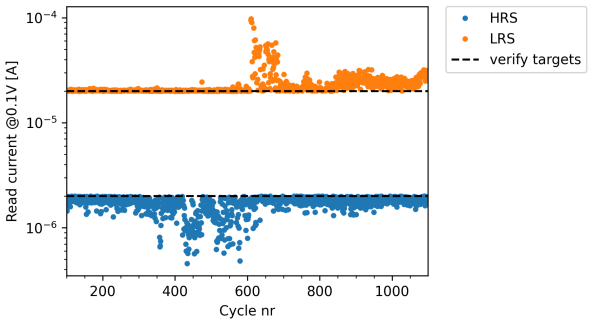


Figure 1. cycling endurance plot showing final SET (LRS) and RESET (HRS) states for 1000 cycles using write-verify programming. The sustained overshooting of LRS target from cycle 600 onwards suggests a transition in the switching behavior.

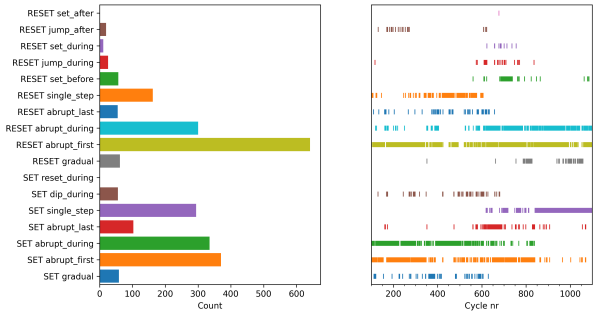


Figure 2. switching curve label assignment corresponding to Fig. 1 cycling. Plot on the left shows the number of observations, and graph on the right indicates at which cycle each event happens.

Amorphous, Highly Conductive Pr0.7Ca0.3MnO3 for Area-Dependent Resistive Switching Devices

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Memristive Pr0.7Ca0.3MnO3 (PCMO) heterostructures exhibit area- dependent resistive switching via a valence change mechanism, making them promising for neuromorphic architectures [1]. A major challenge in PCMO-based memory is higher-dimensional lattice defects that affect oxygen-vacancy migration and concentration. This study mitigates these defects using highly conductive amorphous PCMO fabricated via a CMOS back-end-of-line-compatible process [2] and compares it with low- conductive amorphous and polycrystalline PCMO. The resistance differences are attributed to changes in electronic mobility, based on the analysis of short- and long-range order, Mn–O hybridization, and Mn valence state. AlOx/PCMO devices showed the highest ON/OFF ratio compared to low-conductive amorphous and polycrystalline PCMO, because the field-accelerated oxygen vacancy movement switches the mechanism from Poole–Frenkel emission in the LRS to trap-assisted tunneling in the HRS. The mechanism change was identified by systematically analyzing the I-V asymmetry, device band diagrams for different PCMO types, and shape changes in the I-V curve fits. The band diagrams were calculated from the measured band gaps and work functions of the different PCMO types. Analysis of the electric field distribution in the devices showed a clear correlation between the pre- switching field strength in AlOx and the resulting ON/OFF ratio.

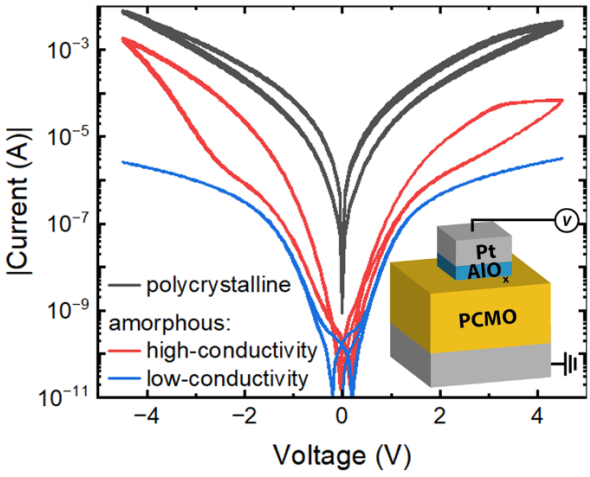


Figure 1. Highest on/off ratio for quasi-amorphous PCMO/AlO_x devices compared to crystalline or amorphous PCMO

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Talks

Spiking Behavior

Memristor-based Parallel-Synapse Leaky Integrate-and-Fire Neuron Circuit for Non-Periodic Spiking Data Processing

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Neuromorphic computing has emerged as a promising approach to overcome the memory bottlenecks and high energy consumption associated with conventional von Neumann architectures. In this study, we develop a hybrid memristor-based neuromorphic system that integrates a volatile Pt/V/AlOx/Pt threshold switching memristor (TSM) as an artificial neuron and a non-volatile Ta/ZrOx/Pt resistive switching memristor (RSM) as an artificial synapse. The TSM-based neuron circuit successfully implements leaky integrate-and-fire (LIF) behavior with adjustable synaptic weights and temporal coding capabilities. Meanwhile, the RSM synapses exhibit stable multilevel resistance states and excellent retention characteristics, enabling long-term storage of synaptic conductance.

By coupling the neuron circuit with multiple artificial synapses, the membrane potential (VM) is shown to depend on both the magnitude and temporal distribution of input signals, allowing precise control of spike generation. Furthermore, the TSM-based neuron operates as an efficient spike encoder, where either the firing frequency or the time-to-first-spike (TTFS) can be directly tuned by the input signal amplitude. This multifunctional capability enables the same hardware unit to perform both neural computation and analog-to-spike signal conversion. The proposed system reproduces key neuronal functionalities, including subthreshold integration, temporal summation, and synchronized firing, highlighting its potential for scalable and energy-efficient neuromorphic hardware applications.

Figure 1. Schematic diagram of LIF neuron circuit and LIF characteristics measured at a fixed input voltage of –8 V with varying RL values from 10 to 39 kΩ.

Figure 2. Schematic diagram showing spatio-temporal signal processing enabled by the parallel-synapse neuron circuit and experimental results for non-periodic spiking information processing.

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Material-Intrinsic Synapse-Like Plasticity and Leaky Integrate-and-Fire Dynamics in a Quasi-One-Dimensional Molecular Memristor

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Memristors are promising building blocks for neuromorphic hardware because their nonlinear and history-dependent responses can emulate essential features of biological synapses and neurons. In particular, molecular and correlated-electron memristors offer a unique opportunity to exploit material-intrinsic dynamics, rather than relying solely on complex circuit design, to generate neuromorphic functions. We focus on the quasi-one-dimensional halogen-bridged metal complex $[Ni(chxn)_2Br]Br_2$ (chxn = cyclohexanediamine), which has recently been shown to exhibit memristive behavior characterized by pinched hysteresis loops, negative differential resistance, and colossal emergent inductance [1]. These features suggest that the slow internal state dynamics responsible for memristive switching may also be used as a physical resource for synapse- and neuron-like operation.

First, we demonstrate synapse-like plasticity using paired current pulses. Two successive current pulses were repeatedly applied to the molecular memristor while varying the pulse interval Δt. The output response strongly depended on the pulse history: as Δt became shorter, the difference between the first and second responses became more pronounced (Fig. 1). This behavior indicates that the device retains a transient memory of the preceding stimulus through its intrinsic relaxation dynamics, resulting in frequency-dependent synapse-like plasticity.

Second, we investigate neuron-like operation based on leaky integrate-and-fire dynamics. Consecutive current pulses were applied to a simple circuit in which the molecular memristor was connected in parallel with an external capacitor. The output response gradually integrated the input stimuli while also exhibiting leakage. When the accumulated response exceeded a threshold, a spike-like firing event was generated (Fig. 2). This behavior corresponds to leaky integrate-and-fire dynamics, a fundamental model of neuronal excitation.

These results demonstrate that $[Ni(chxn)_2Br]Br_2$ can reproduce both synapse-like plasticity and neuron-like firing within a minimal device/circuit configuration. Importantly, the observed functions are not imposed by sophisticated external circuitry, but arise from the intrinsic nonlinear and time-dependent dynamics of the molecular memristor. Our findings suggest that molecular memristors can serve not only as nonvolatile memory elements but also as active dynamical components for compact neuromorphic hardware. More broadly, this material-driven approach provides a promising route toward energy-efficient computing devices based on correlated molecular systems.

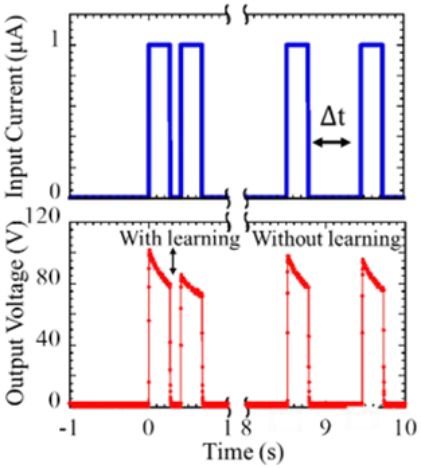


Figure 1. Synapse-like plasticity in $[Ni(chxn)_2Br]Br_2$. Paired current pulses with different pulse intervals Δt are applied to the molecular memristor, and the output response exhibits history- and frequency-dependent plasticity.

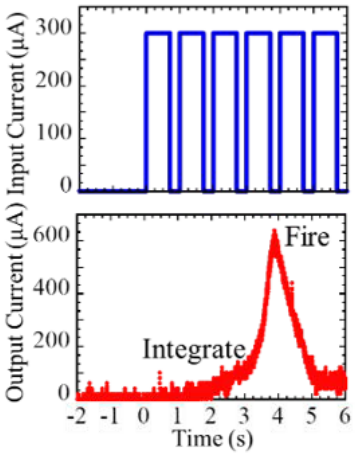


Figure 2. Neuron-like leaky integrate-and-fire dynamics in $[Ni(chxn)_2Br]Br_2$. Consecutive current pulses are applied to a circuit consisting of the molecular memristor and an external capacitor, leading to integration, leakage, and spike-like firing.

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Multimodal Memristive Blinking Neurons for Ultra-High Density Spiking Neural Networks

Yue Zhou[1], Zelin Ma[1], Yuetong Fang[1], Hanxiao Liu[1], Raphael Gisler[2], Haotian Fu[1], Alexandre Bouhelier[3,4], Juerg Leuthold[2], Bojun Cheng[1]

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The continued scaling of neural networks demands compute-in-memory (CIM) hardware with ultra-dense, highly parallel processing. Optoelectronic architectures have emerged as a promising platform for large-scale neuromorphic systems owing to their high bandwidth and flexible connectivity [1-2]. However, their scalability is fundamentally challenged by diffraction-limited readout strategies [3-4]. Here we demonstrate a multimodal memristive blinking neuron (MMBN). Driven by atomic-scale filament dynamics, the MMBN executes intrinsic integrate-and-fire operations with photonic spike emission [5]. This co-integration eliminates the need for bulky peripheral circuits, shrinking the neuron pitch to 1 μm. The MMBN further leverages wavelength and polarization to encode information under high-density integration. By multiplexing multiple distinguishable channels within a diffraction-limited optical spot, the proposed approach decouples communication capacity from spatial resolution, enabling substantially higher information density within a fixed footprint.

The MMBN features a volatile Ag/PMMA/Ag memristive structure where the electrodes are engineered into anisotropic plasmonic bow-tie antennas strongly confining and enhancing the localized electric field. The leaky-integrate-and-fire (LIF) neuronal behavior is efficiently merged with nanoscale photon emission during the dynamic growth and rupture of atomic filaments. The anisotropic antenna strictly guarantees linear polarization (Fig. 1a). By engineering the layout orientation of these antennas, the polarization states can be deterministically defined (Fig. 1b, 1c). Furthermore, the MMBN exhibits voltage-tunable emission wavelengths (Fig. 1e, 1f, 1g). The emission shifts from 770 nm (∼1.61 eV) at 6 V to 640 nm (∼1.94 eV) at 10 V (Fig. 1h). We tentatively attribute this blue shift to the Stark effect, where the external field modulates internal state asymmetries to widen the energy gap. Through the synergistic encoding of wavelength and polarization channels, the MMBN transforms the classical optical spike output spike(t) into a multidimensional state spike(t,λ,p).

Leveraging this multi-dimensional multiplexing, we selected 6 V and 10 V to access two distinct wavelength channels. Because varying voltage amplitudes inherently alter the integration rates (Fig. 2a, 2b), we introduce heterogeneous fast and slow neuron models with their respective thresholds. We constructed a MMBN-based heterogeneous Spiking Neural Network (MMBN SNN) comprising two convolutional and two fully connected layers (Fig. 2d). In the proposed hardware implementation, the output layer can be mapped onto a high-density 2x2 MMBN array within an ultra-compact ∼0.5 μm^2 footprint (Fig. 2c). By pairing orthogonal antenna orientations for adjacent cells with row-specific voltage drives, the system guarantees complete state separability. This design allows the micron-level spot to be demultiplex into four independent channels via filters and polarizers at the receiving end. The network yields a 97.93% simulated accuracy on a 4-class MNIST classification task (Fig. 2e, 2f, 2g). By exploiting diffraction-limited optical overlap for multichannel communication, MMBN overcomes the fundamental density bottleneck, providing a highly scalable hardware solution for next-generation neuromorphic platforms.

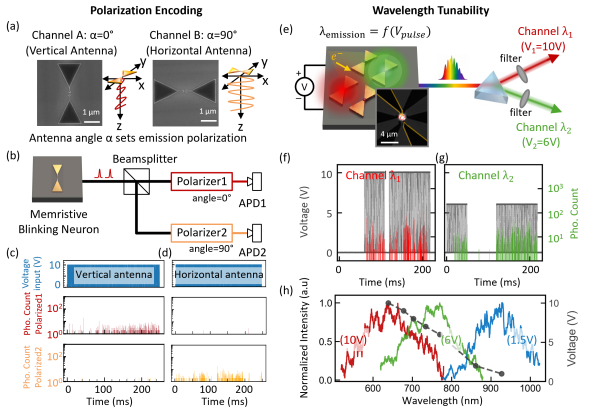


Figure 1. Polarization encoding and wavelength tunability of the memristive blinking neuron. (a) Scanning electron microscopy (SEM) images and the xy-plane polarization states of vertical (α=0°) and horizontal (α=90°) bow-tie antennas. (b) Schematic of the experimental setup. Light emitted from the MBN is divided into two optical paths by a beam splitter. Each path passes through a linear polarizer before being detected by an avalanche photodiode (APD). (c, d) Measured optical intensities when the two polarizers are oriented orthogonally (0° and 90°). Vertical antenna emission is only detected in the 0° aligned channel, and horizontal antenna emission is detected in the 90° aligned channel, indicating strong orthogonal polarization isolation. (e) Demonstration of wavelength demultiplexing in a 2x2 array. The central inset displays a microscope image of two simultaneously activated diagonal devices. By applying different voltage amplitudes, the overlapped emission spots can be decoupled into two independent channels using filters. (f, g) Measured optical intensities of Channel λ_1 and Channel λ_2, driven by 10 V and 6 V applied voltages, respectively. Left axis: Input voltage (black). Right axis: Photon counts per 100 µs (red and green), demonstrating successful signal decoupling. (h) Voltage-tunable emission. Left axis: Electroluminescence spectra measured with different pulse amplitudes (1.5 V in blue, 6 V in green, 10 V in red). Right axis: Extracted center wavelength versus applied pulse amplitude, illustrating a blue shift with increasing voltage.

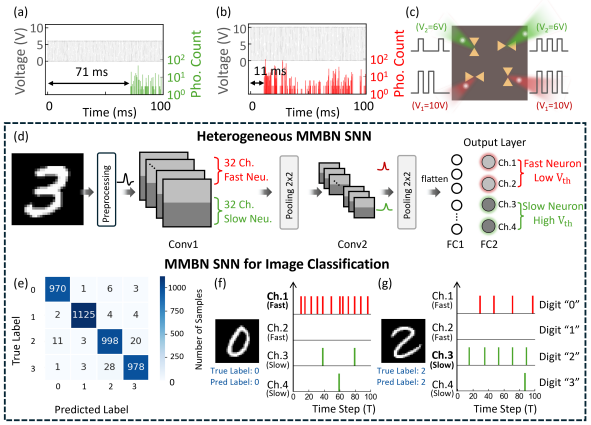


Figure 2. Device integration dynamics and the heterogeneous MMBN SNN architecture. (a, b) Integrate-and-fire dynamics of the MMBN under varying voltage amplitudes. Stimulated by identical 1 kHz pulse trains, the device requires 71 pulses at 6 V (a) and 11 pulses at 10 V (b) to trigger photonic spikes. (c) Hardware implementation of multidimensional multiplexing via orthogonally oriented adjacent antennas and a row-specific programming voltage strategy. (d) The heterogeneous MMBN SNN architecture, comprising a preprocessing layer, two spiking convolutional layers, and two fully connected layers. Each convolutional layer evenly allocates the channels to fast and slow neurons. The final output layer consists of 4 neurons corresponding to the 4-classification targets. (e) Simulated confusion matrix for the 4-class MNIST classification task. (f, g) Simulated inference examples for digit "0" and digit "2". The highest photon firing rate is obtained for the digit as predicted.

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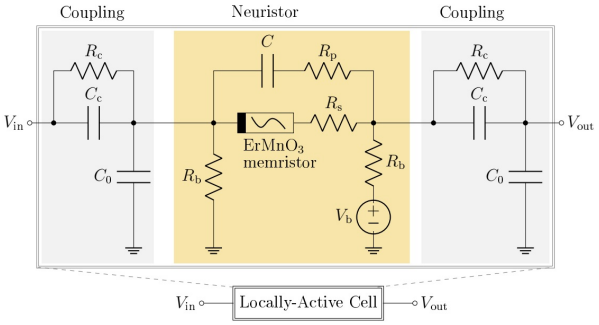
A Spiking Memristive Neuristor Chain at the Edge-of-Chaos

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In this contribution, we propose a memristive neuristor circuit capable of propagating single-event neural spikes along chains, crossings and circles, mimicking the leaky-integrate-and-fire behavior of biological neurons. Inspired by the neuronal axon structure and couplings at the nodes of Ranvier, the novel circuit structure implements a neuristor circuit based on a locally-active volatile memristive device and resistive-capacitive couplings as sketched in Fig. 1. Employing precise, compact models of Pt/ErMnO3/Pt memristor - which where experimentally validated in our previous works [1,2] and exhibit local activity within their negative differential resistance (NDR) range - we demonstrate in this paper that the coupling of multiple devices can lead to the propagation of single-pulse events along a chain of these locally active cells. Therefore, we have studied under which coupling conditions assuming the single cell circuit is biased on the Edge-of-Chaos, meaning it is locally active but stable, passes neuronal-like signals, triggered by external pulse inputs, unidirectionally to the next cell. For example, Fig. 2 showcases a three-way crossing with chains of five cells illustrating inhibitory (no pass) and exhibitory (pass) propagation dependent on the spike time delay. Our results obtained so far, reveal the biasing conditions of the internal temperature-driven device mechanism for long-term stable operations in the NDR region, robustness when incorporating internal temperature state noise and the possibility to modulate the spike propagation through non-volatile memristive couplings. Simulations were performed in the open-source NgSPICE environment enabling reuse by the research community. Our work shows that not only thermally-driven memristors but also CMOS-based 2T1RC [3] or simple thyristor circuits can mimic this neuronal spike propagation which hence offers a promising way to realize sparse energy-efficient spiking neural networks employing classical non-volatile memristive crossbar arrays while omitting analog-to-digital signal conversion.



V_b, R_b bias the locally-active memristor in its NDR at the Edge-of-Chaos, which exhibits a R_p-R_s-controlled spike waveform discharging C when triggered by inputs at V_{in} or V_{out} from neighboring cells through the couplings R_c, C_c while C_0 controls the refractory.

Figure 1. Locally-active (LA) neuristor cell with couplings on both sides emulating leaky-integrate-and-fire neurons in an axon chain.

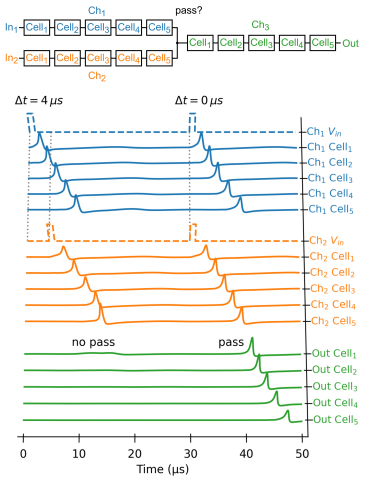


Figure 2. Three-way crossing behavior of coupled LA neuristor chains showing delay dependent signal passing.

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Electronic Pain Perception Enabled by Ag/CeO_2 Diffusive Memristors

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Volatile threshold-switching memristors based on diffusive metal-ion dynamics provide a powerful hardware platform for bio-inspired neuromorphic systems, particularly artificial pain perception devices that emulate biological protective responses. Herein, we report Ag/CeO_2/ITO diffusive memristors and investigate their potential for realizing electronic pain perception through threshold-driven neuronal functionalities. The memristors consist of an amorphous CeO_2 thin film as the switching layer, sandwiched between an ITO bottom electrode and an Ag top electrode, in which threshold switching arises from field-driven Ag-ion migration, reduction, and spontaneous filament dissolution. By systematically varying the CeO_2 thickness, forming-free operation was achieved in thinner devices (30 and 50 nm), whereas thicker devices (100 and 150 nm) required electroforming due to increased ion-migration barriers. All devices exhibit volatile threshold switching with ultralow leakage current, large ON/OFF resistance ratios exceeding 10^2–10^4, narrow threshold voltage distributions, and excellent cycle-to-cycle and device-to-device uniformity.

The optimized memristor was exploited to emulate key pain-perception functionalities under electrical pulse stimulation. The device remained inactive under subthreshold stimuli while producing abrupt firing above a critical threshold, demonstrating clear threshold perception. Repeated subthreshold pulses induced temporal summation and firing, mimicking neuronal integration. The intrinsic relaxation dynamics enabled memory decay and recovery, resembling the transient response of biological sensory neurons. Furthermore, exposure to high-intensity stimuli induced sensitization effects, including reduced firing thresholds and enhanced responses, analogous to biological hyperalgesia and allodynia. Notably, the device exhibited non-adaptive behavior, continuously responding to repeated noxious stimuli, a defining characteristic of biological pain receptors.

The observed threshold response, relaxation dynamics, sensitization, and non-adaptive behavior collectively demonstrate the ability of the Ag/CeO_2/ITO diffusive memristor to reproduce essential features of biological pain perception within a single device architecture. Unlike conventional sensing and computing systems that require separate units for signal acquisition, processing, and memory storage, the proposed memristive platform inherently integrates these functionalities, enabling low-power and hardware-efficient operation.

This work highlights the potential of Ag/CeO_2/ITO diffusive memristors as compact and energy-efficient electronic pain perception devices. The demonstrated biomimetic functionalities establish a promising pathway toward intelligent neuromorphic hardware capable of autonomous environmental awareness, adaptive response, and next-generation bio-inspired sensory computing.

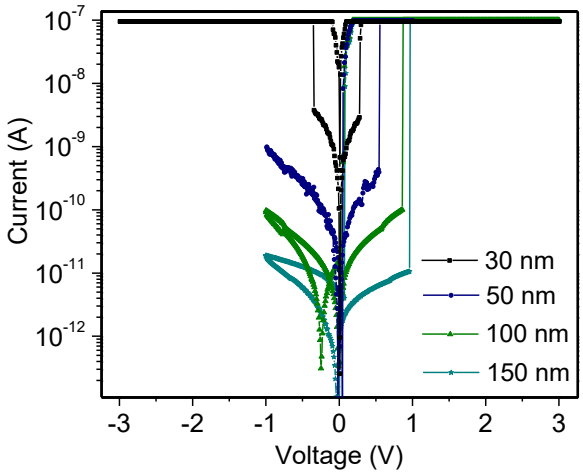


Figure 1. Current–voltage (I–V) characteristics of Ag/CeO_2/ITO diffusive memristors with different CeO_2 thicknesses, demonstrating volatile threshold-switching behavior.

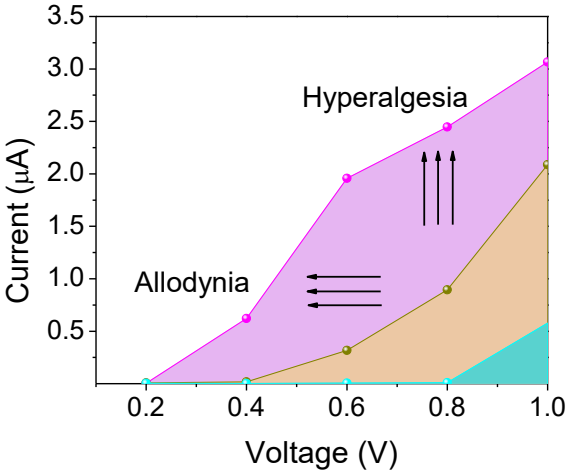


Figure 2. Experimental emulation of hyperalgesia and allodynia in the artificial pain perception system through stimulus-induced sensitization.

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Talks

Integration / Design

Energy-Efficient Edge Systems via Emerging Memory Co-Integration

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The shift from cloud-based data classification toward edge computing has enabled real-time data processing closer to the source of data collection, cutting latency and improving overall efficiency. Yet this shift brings with it strict demands around power consumption, physical footprint, and computational performance. Meeting these demands calls for novel hardware approaches that can operate within such tight constraints.

Incorporating emerging memory technologies at the back-end-of-line (BEOL) of CMOS circuits, or within 3D array configurations, opens up exciting possibilities for advancing neuromorphic hardware.

This presentation highlights the importance of design-technology co-optimization (DTCO) as a means of seamlessly combining emerging memory devices with CMOS circuits, laying a design foundation for next-generation memory systems built on BEOL and 3D integration. It will explore the challenges and opportunities that arise when co-designing devices, circuits, and architectures together, making the case for a co-development approach to enabling the full potential of computing at the edge.

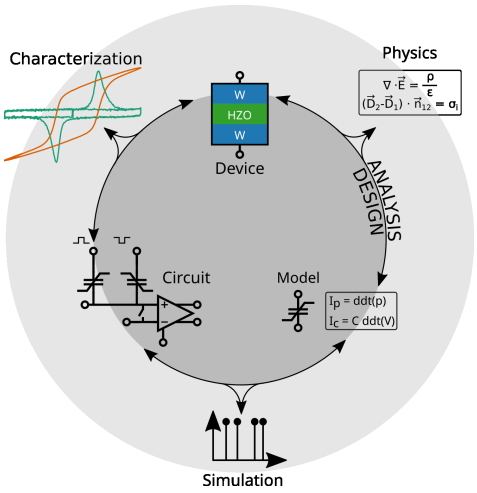


Figure 1. Design-Technology Co-Optimisation framework

Noise-Enhanced Synaptic Weight Adaptation in HfO_2 Memristive Synapses

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Memristors have emerged as promising candidates for neuromorphic computing due to their ability to emulate synaptic functionalities such as analog conductance modulation and spike-timing-dependent plasticity (STDP) [1], [2]. While stochastic switching behavior is traditionally regarded as a source of variability, biological neural systems demonstrate that noise can play a constructive role in learning and information processing. In STDP, the evolution of synaptic weight depends on the temporal correlation between pre- and post-synaptic spikes. Under weak excitation conditions, however, conductance modulation can become insufficient, limiting the effectiveness of weight updates. Stochastic resonance (SR), in which an optimal amount of noise enhances a weak signal, offers a potential mechanism for improving synaptic adaptation [3], [4]. Motivated by this, the present work explores whether noise-assisted switching can be harnessed to enhance STDP-based learning in HfO_2-based memristive synapses across multiple conductance states, thereby facilitating weight adaptation.

The schematic of our HfO_2-based memristor device is shown in the inset of Fig. 1(a), with the top and bottom contacts, and the switching layer indicated accordingly. The devices were initially characterized without any external noise input with bipolar sweep input; the corresponding current-voltage (I-V) characteristics are shown in Fig. 1(a) (the inset shows the applied input). Experimental measurements for STDP were performed by varying the time delay between pre-synaptic [see Fig. 2(a), (e)] and post-synaptic pulses [see Fig. 2(b), (f)], thereby generating effective pulses having different widths [see Fig. 2(c), (g)] by maintaining the same sub-threshold amplitude. The corresponding output current is shown in Fig. 2(d) and (h).

In the absence of external noise (σ_N = 0 mV) in the set pulse of the pre-synaptic input at sub-threshold conditions [as shown in Fig. 2(a), (e)], negligible conductance modulation was observed for all delay conditions at σ_N = 0 mV [see Fig. 1(b) and Fig. 2(d), (h)]. Here, the delay between the pre and post-synaptic pulse plays a crucial role. A larger pulse width is achieved with lower delay; increasing the delay yields smaller pulse width. After adding Gaussian noise with different noise intensities (σ_N) to the set pulse of the pre-synaptic input, a pronounced enhancement in the resistance ratio (R_{off}/R_{on}) is observed, for optimal noise intensities, yielding several conductance values [see Fig. 1(b)].

The optimal noise intensity was found to depend strongly on the effective pulse width, with longer pulse durations requiring lower noise intensities and producing larger conductance modulation than shorter pulses. For a spike-timing delay of 4 ms, the effective pulse width is larger, enabling stochastic resonance (SR) to occur at a relatively low noise intensity of $\sigma_N \approx 40$ mV. As the delay increases, the effective pulse width reduces, resulting in higher optimal noise intensity for the SR condition. Further increases in noise intensity degrades the performance of the device and reduce conductance modulation, as shown in Fig. 1(b).

The results reveal that the effective pulse width generated by STDP plays a critical role in determining the stochastic resonance response in the memristive device. As a consequence, different spike-time delays require different optimal noise intensities to yield distinct conductance modulation levels under identical input conditions. This behavior enables delay-controlled synaptic weight tuning in a single HfO_2 memristive synapse. Furthermore, since stochastic resonance is known to enhance the detection and transmission of weak signals in biological neural systems, the observed noise-assisted conductance modulation may facilitate synaptic adaptation even under weak firing conditions or at larger pre- and

post-synaptic delays, where deterministic switching becomes less probable. These findings highlight the potential to exploit stochasticity as a functional resource for implementing robust, adaptive neuromorphic learning in compact memristive hardware.

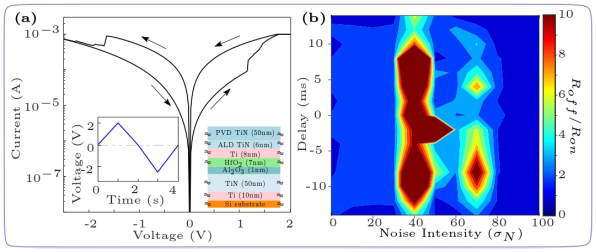


Figure 1. (a) I –V characteristics of the memristor, without external noise input. Insets show the applied input, and the schematic of the device structure. (b) Off-to-on resistance ratio (R_{off}/R_{on}) as a function of noise intensities, for different delays.

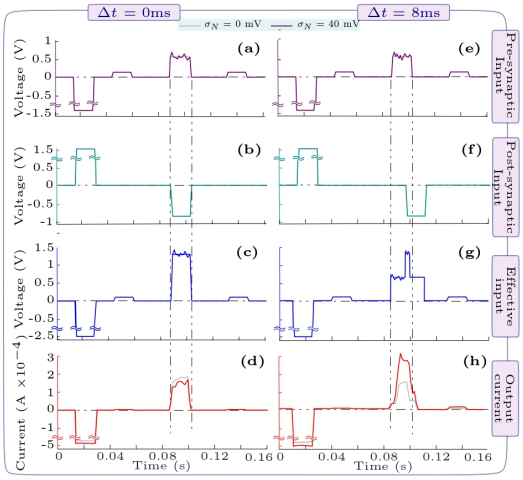


Figure 2. (a)-(d)/[(e)-(h)] Delay (Δt) = 0 ms/[8 ms]: (a)/[(e)] Pre-synaptic input, (b)/[(f)] post-synaptic input, (c)/[(g)] effective input, and (d)/[(h)] corresponding output current. Gray trace shows the corresponding inputs and outputs without noise.

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Automated Statistical Validation Framework for Memristor-Based Random Number Generators Using NIST SP 800-22

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Memristor-based true random number generators (TRNGs) have emerged as promising candidates for hardware security applications due to their ability to exploit stochastic phenomena such as random telegraph noise (RTN), filamentary fluctuations and volatile switching dynamics [1, 2]. However, the development of these devices requires efficient statistical validation of the generated bitstreams.

In this work, we present an automated framework for evaluating memristor based entropy sources using the complete NIST SP 800-22 statistical test suite [3]. The proposed platform enables parallel execution of independent tests and provides near real-time statistical feedback while maintaining compatibility with the original NIST methodology.

The framework was developed to support ongoing research on memristor-based entropy sources and facilitates the comparison of binary sequences generated under different experimental conditions. Experimental validation demonstrated full agreement with the official NIST implementation while reducing the overall execution time to approximately 1.75 s for the recommended set of 55 sequences of 1 Mbit each.

The proposed approach is particularly suitable for studies involving RTN-based TRNGs and other stochastic memristive phenomena requiring repeated generation and validation of random sequences. By simplifying the randomness assessment process, the framework provides a practical tool that can accelerate the development and characterization of future memristor-based hardware security systems.

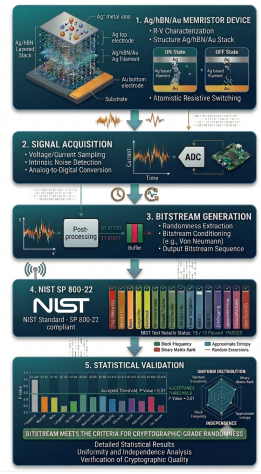


Figure 1. Workflow for Statistical Validation of Memristor-Based Entropy Sources

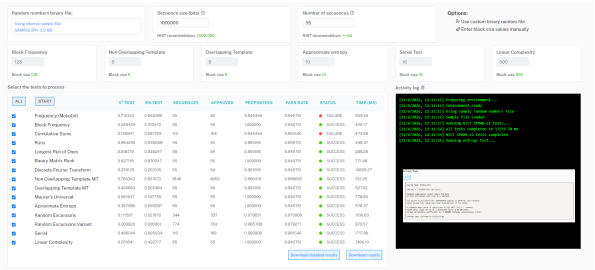


Figure 2. Graphical User Interface of the Proposed Statistical Validation Framework.

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Correlating the impact of structure, morphology and the defects of the solution-processed tungsten oxide on RRAM devices for PUF applications

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Cybersecurity is becoming a growing concern with the recent boom in information technology. Unsecured data transmissions can be easily tampered with or stolen for malicious purposes as connectivity in fields such as health, entertainment, and military becomes unavoidable. Hence, Physically Unclonable Functions (PUFs) are considered the optimal solution due to their unpredictability, which originates in hardware components such as transistors, logic gates, and memristors. Among these devices, resistive random-access memory (RRAM), a type of memristor, is emerging as an ideal candidate for PUF implementation due to its inherent temporal and spatial variations. The current work correlates the effects of structure and defects on tungsten oxide (WOx)-based RRAM devices, as this is a crucial parameter for narrowing the effective conditions for RRAM-based PUF. Furthermore, the solution-processing route used in this work offers a cost-effective, facile method for studying RRAM-based PUFs for security applications. Additionally, the solution-processed WOx films are especially attractive due to their inherent stochasticity. The RRAM devices exhibited good endurance (10^3 cycles) and retention times (10^3 s), which offer consistent, stable, and reliable PUFs. It is evident from the PUF performance metrics observed with WOx samples annealed at 400 °C/ 1h. The uniformity (50 %), bit-error rate (0%), diffuseness (47.62%), and uniqueness (48%) are observed to be close to their respective ideal values. Hence, the study demonstrates the structure and the impact of defects on the performance of RRAM devices and also paves the way for cost-effective RRAM-based devices for PUF applications.

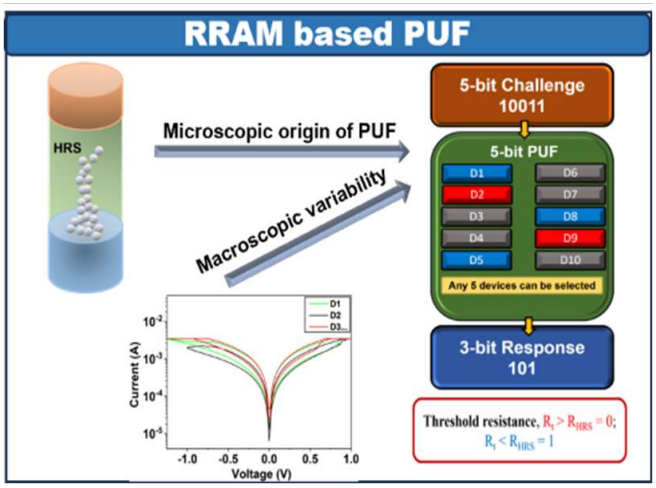


Figure 1. Schematic representation of solution-processed WOx based RRAM devices employed for PUF application

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Electrochemical Polishing Approach for Reliable Quantum Memristors

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Memristive devices have significantly developed in the last decade, expanding their application horizon much beyond memory applications. Especially important is their functionalities as artificial neurons and synapses, making them promising building units for the next generation bio-inspired neuromorphic hardware. However, other applications such as selectors, HF switches and sensors are also intensively studied and reported. Recently, we demonstrated a new application of memrsitors using the quantum conductance levels as standard for resistance in accordance with the new directions given by SI [1]. Here the main challenge was to stabilize the quantum conductance levels over time for reliable comparison/verification.

In this contribution the main criteria for selection of materials systems for quantum memristors will be discussed. The advantages and disadvantages of different switching layers and active electrodes will be highlighted in terms of selection criteria for obtaining reliable QPC. Effects of impurities and protons in the processes and stability of the resistances will be critically overviewed.

The method of electrochemical polishing will be introduced, that allows to ensure stable, reproducible and adjustable quantum point contacts. The fundamentals of this procedure will be explained and its application to nanoscale electrochemical memristive devices will be will be critically discussed.

Justification and the main principle of using the QPC as a standard for resistance will be provided. Different approaches for stabilization of the quantum steps with low number of participating atoms (5 <) will be shown. Fundamental materials principles and processes will be highlighted.

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Talks

Circuit Design

From Compute-in-Memory to New Frontiers

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Memristive devices, and in particular resistive random-access memories (RRAMs), are widely discussed as promising building blocks for compute-in-memory architectures. Their non-volatility, high density, multi-level capability, and ability to combine storage and computation make them attractive candidates for neural network inference, matrix-vector multiplication, and other data-intensive workloads. Consequently, much of today's architectural discussion around memristors is centered on accelerating artificial intelligence by reducing data movement across the memory hierarchy.

This invited talk takes this established view as a starting point, but deliberately looks beyond it. It argues that memristors should not be understood as "better memories" or as mere analog accelerators for neural networks. Instead, they form a technology class whose device-level properties can be exploited across several layers of computing systems, from ultra-low-power embedded architectures to reconfigurable fabrics and reliable systems for harsh environments.

A central challenge in this broader view is the gap between device physics and system architecture. Memristive devices exhibit stochastic switching, variability, drift, endurance limits, and complex dependencies on programming conditions. These properties cannot be ignored when evaluating complete systems. Therefore, the talk first introduces modeling and virtual prototyping as key enablers for architecture exploration. Using variability-aware, measurement-driven models and SystemC-based simulation, memristive subsystems can be analyzed not only as isolated devices, but as components embedded into realistic computer architectures. Example applications include non-volatile register files and caches, analog in-memory neural computation, radiation-resilient memory subsystems, RISC-V processors with integrated RRAM, and variability-tolerant analog neuron circuits.

Building on this foundation, the talk then discusses two current research directions that move memristors into new architectural roles. The first is the use of multi-level RRAM as dense non-volatile configuration memory for multi-context FPGAs. Here, memristors enable multiple hardware contexts to coexist on the same reconfigurable fabric, supporting fast runtime context switching, normally-off operation, and new trade-offs between flexibility, area, and energy. The second direction is the use of RRAM-based subsystems in Low Earth Orbit missions and other harsh environments. Temperatures well below freezing do not noticeably impair the switching behavior of RRAMs, which makes them well-suited for use in orbit. In this scenario, non-volatility, radiation tolerance, checkpoint memory, and in-memory support for error correction become central design aspects for reliable and energy-efficient spaceborne computing.

Overall, the talk presents memristors as a bridge between memory, computation, reconfiguration, and resilience. Compute-in-memory remains an important application, but it is only one part of a much larger design space. The main message is simple: memristors are not just memory devices. They are architectural building blocks for future computing systems.

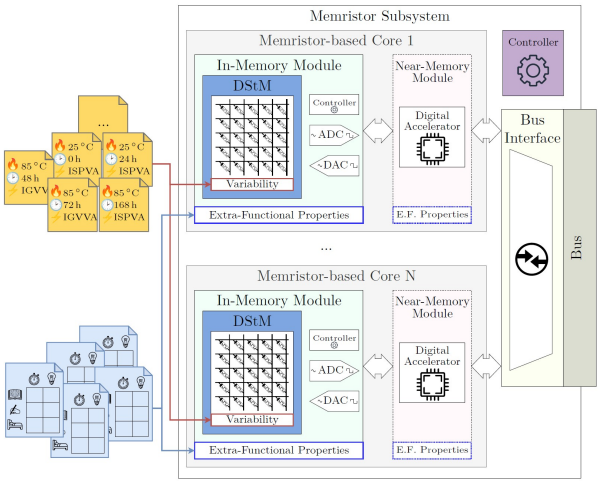


Figure 1. Block diagram of the MeSSi virtual prototyping platform

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From MAGIC to PyPIM: The Evolution of Abstraction in PIM

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Processing-in-Memory (PIM) promises to overcome the limitations of the von Neumann architecture by reducing data movement and bringing computation directly into memory. Over more than a decade, the ASIC[2] group at the Technion has explored this vision in the context of digital PIM and stateful logic, spanning multiple levels of the computing stack, from emerging memory devices and logic-in-memory architectures to programming models and software abstractions. This talk reviews that journey and highlights how successive advances in abstraction transformed PIM from device-level logic-in-memory primitives into a programmable computing platform.

Our early work established the foundations of logic-in-memory using emerging non-volatile devices. Building on approaches such as IMPLY and MRL, we introduced MAGIC, a scalable approach for performing logic directly within memristive memory arrays. We subsequently developed techniques for mapping arithmetic and computational kernels to in-memory operations, execution mechanisms including the memristive Memory Processing Unit (mMPU), and optimization frameworks such as SIMPLER and X-MAGIC. These efforts demonstrated that complex computations, ranging from arithmetic operations to neural-network inference and sorting, can be efficiently executed inside memory, while exposing the growing challenge of programmability.

The main focus of this talk is the evolution of PIM abstraction. As PIM architectures matured, programmability emerged as a central challenge. Our research progressed through several generations of abstraction, moving responsibility from the programmer into the compilation and execution infrastructure.

The first generation focused on hiding device-specific details. Using logic-synthesis tools such as ABC, hardware-independent combinational functions were translated into sequences of primitive in-memory operations and executed by controllers such as the mMPU. This approach enabled computations to be expressed independently of the underlying memory device while still relying on low-level execution mechanisms.

The second generation introduced AbstractPIM, which added an intermediate hardware-independent representation between architectural instructions and device-level micro-operations. This additional abstraction layer decoupled architectural functionality from specific PIM technologies and enabled systematic optimization and portability across different implementations.

A third generation, first introduced in PIMDB and built around an extended mMPU architecture, shifted the abstraction boundary altogether. This architecture exposes a richer PIM ISA to the programmer while encapsulating complexity within a programmable microcoded execution engine. Support for loops, conditional execution, and parameterized control flow enables a single microcode implementation to realize the same ISA operations across varying operand widths. The same microcode can often be reused by multiple related instructions, substantially reducing the need for instruction-specific micro-operation generation. Later work demonstrated that many of these capabilities could be realized either in dedicated hardware or through a software driver, further decoupling the programming model from the underlying implementation.

Finally, PyPIM builds upon this execution model to provide a Python-inspired programming interface. By translating familiar software constructs into PIM operations, PyPIM enables application developers to exploit in-memory computation without requiring expertise in memory arrays, instruction formats, or device technologies.

From MAGIC to PyPIM, this journey reflects a continuous effort to raise the abstraction level of processing-in-memory systems, transforming device-level logic-in-memory primitives into a practical, programmable, and technology-independent computing paradigm.

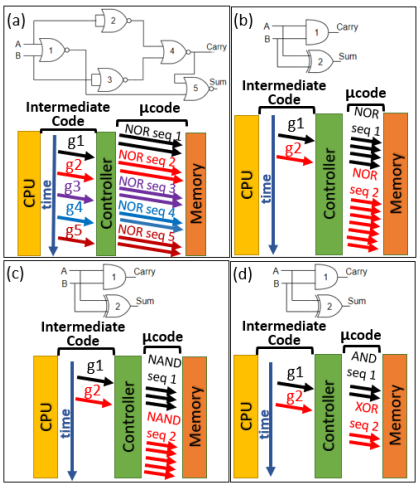


Figure 1. Compilation example for a half adder using various ISAs and target machines: (a) A NOR ISA and MAGIC NOR target machine. (b) All 2-input and single-output ISA and MAGIC NOR target machine. (c) All 2-input and single-output ISA and MAGIC NAND target machine. (d) All 2-input and single-output ISA and 2-input and single-output MAGIC target machine

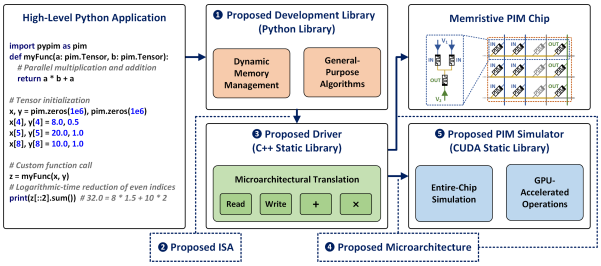


Figure 2. PyPIM end-to-end integration: ❶ Python to PIM-ISA ❸ PIM-ISA to PIM micro-operations

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Precision-Energy Trade-offs in 28nm RRAM-Based MAC Arrays

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Resistive Random-Access Memory (RRAM) has emerged as a promising candidate for neuromorphic edge computing due to its scalability, non-volatility, and native support for in-memory multiply-accumulate (MAC) operations [1]. A key design tradeoff exists: higher LRS resistance reduces bitline current and lowers energy, but increases cycle-to-cycle (C2C) variability and narrows the LRS/HRS window, potentially degrading MAC precision [2]. This work systematically characterises this tradeoff on a 28 nm CMOS-integrated TaOx/Ta RRAM chip through on-chip MAC measurements and VGG16 inference simulations across different LRS targets.

The chip integrates a 15×15 1T1R array in a BEOL process on 28 nm CMOS, with die schematc shown in Fig. 1(a). Devices exhibit stable bipolar switching over 100 cycles with HRS/LRS ratio exceeding 10, confirmed by I-V curves in Fig. 1(b). LRS targets spanning 2 kΩ to 20 kΩ are programmed via read-and-verify (±1% threshold), while HRS is independently fixed at 500 kΩ (10% tolerance). Post-programming filament relaxation introduces excess variability beyond converged targets[3]. CDFs in Fig. 1(c) confirm well-separated LRS distributions against a broad HRS tail. The CoV of LRS states monotically increases from 2.6% at 2 kΩ to 16.1% at 20 kΩ, while HRS exhibits the largest spread at 28.7%.

On-chip MAC accuracy is evaluated by programming random weight matrices and input patterns into a 15×1 column. For each configuration, 1000 random binary input vectors are applied and bitline current measured directly. A reference, expected MAC current, is computed by serially reading cell resistances and analytically summing contributions. Accuracy is quantified via MAE, R^2, and slope of a linear fit to measured versus expected MAC current as demonstrated in Fig. 2 (a-b), and variation of MAE with LRS in Fig. 2(c). At 3 kΩ, high aggregate bitline current produces substantial IR-drop, yielding slope of 0.87 and MAE of 7.4 µA. As LRS increases, IR-drop nonlinearity is suppressed: MAE plateaus near 2.5 µA above 5 kΩ and slope recovers to 0.97 at 20 kΩ. R^2 shows marginal decline at higher targets, reflecting increased C2C variability in MAC distributions.

Experimentally measured LRS and HRS distributions are incorporated into a VGG16 inference simulation on CIFAR-10. Weight magnitudes are bit-sliced and mapped to memristor reads, with '1' bits sampling from measured LRS distributions and '0' bits from the shared HRS distribution. As demosntrated in Fig. 2(d), across the LRS targets and different weight precisions (8, 12, 16 bits), inference accuracy increases monotonically with LRS target: from 72% with 3 kΩ to 75% with 20 kΩ. Despite monotonically increasing C2C variability, accuracy does not degrade as the IR-drop suppression at higher LRS offsets the variability penalty. Inference energy drops 6× from ∼490 mJ at 3 kΩ to ∼85 mJ at 20 kΩ for 16-bit operation as shown in Fig. 2(e).

In summary, on-chip MAC measurements and VGG16 simulations jointly demonstrate that 20 kΩ achieves 75.2% CIFAR-10 accuracy with 6× lower energy than 3 kΩ, establishing higher LRS targets as the superior operating point for RRAM-based edge AI.

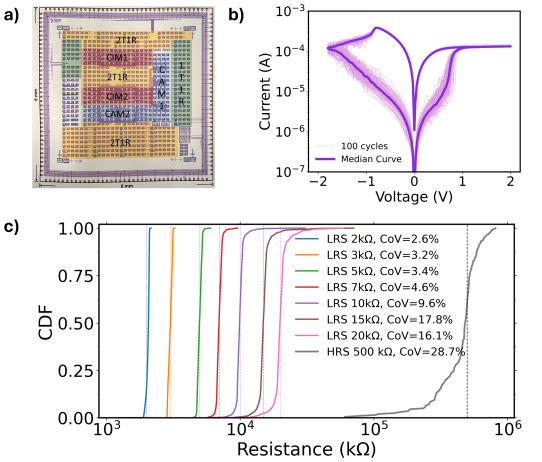


Figure 1. TaOx/Ta RRAM characterisation on 28 nm CMOS. (a) Chip layout; (b) I-V switching curves over 100 cycles; (c) CDFs of all LRS targets and HRS

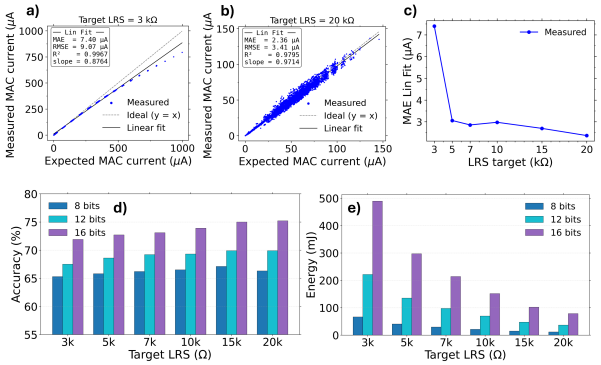


Figure 2. On-chip MAC accuracy across LRS targets. (a–b) Measured versus expected MAC current for 3 kΩ and 20 kΩ, (c) MAE versus LRS target, (d) inference accuracy vs LRS target & (e) inference energy vs LRS target

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Mixture density networks for probabilistic forecasting of resistive switching

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Stochastic resistive switching is a fundamental challenge shared by all filamentary memristive devices: identical voltage pulses applied to the same device can yield markedly different conductance states due to the stochastic nature of conductive filament formation and dissolution [1]. This cycle-to-cycle (C2C) variability fundamentally limits deterministic modeling approaches and hinders the reliable design, simulation, and programming of memristive devices for neuromorphic and analog in-memory computing applications. Accurate probabilistic models of switching behavior would enable stochastic device optimization, worst-case circuit design, and efficient automated characterization workflows.

In this work, HfOx-based memristive devices are used as demonstrators to develop and validate such a framework, using mixture density networks (MDNs). The MDN learns the stochastic switching behavior directly from voltage-pulse measurements: rather than predicting a single conductance value, the MDN outputs the full probability distribution of achievable post-pulse conductance states given pulse polarity, pre-pulse conductance, and applied voltage. This enables the model to capture multimodal switching behavior that conventional deterministic models fundamentally cannot represent.

Trained and evaluated on experimental data, the MDN is able to capture unimodal distributions observed for low and high, set and reset voltage-pulses and the multimodal distributions arising at voltages pulses in between (Fig. 1 and 2). Model performance is quantified using the coefficient of determination R2 and the continuous ranked probability score (CRPS). The MDN achieves R2 = 0.95, explaining 95 % of the observed variance in post-pulse conductance, and a CRPS of 4.8 µS, indicating well-calibrated predictive distributions to resolve the C2C-variability. The CRPS result indicates that the actual measured value will typically fall within the predicted distribution with an average calibration error of 4.8 µS. The MDN already captures the dominant switching statistics with as few as 40 training samples, confirming the data-efficiency of the approach. The proposed framework demonstrates how probabilistic data-driven models can enable data-efficient and variability-aware modeling of emerging nanoelectronic devices. Furthermore, the MDN-framework is automatable and can be directly implement into applications. This is demonstrated by the application in a training algorithm for single-layer artificial neural networks, where the MDN serves as an estimator for realistic voltage and conductance-dependent C2C-variability.

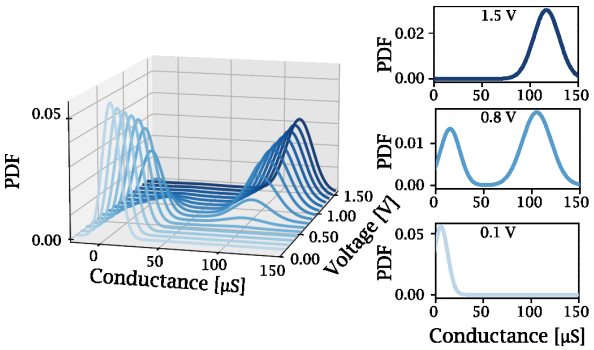


Figure 1. MDN-predictions of conductance distributions across different set voltages. Set predictions are unimodal for HRS and LRS and multimodal at intermediate voltages.

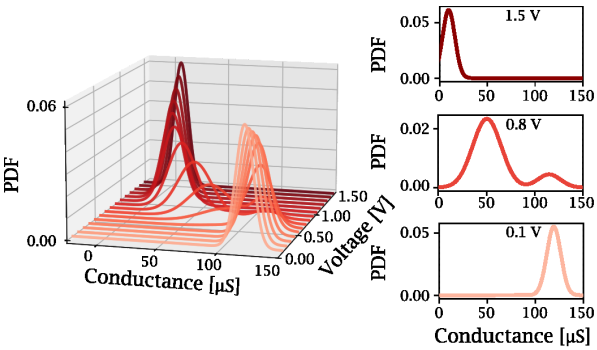


Figure 2. MDN-predictions of conductance distributions across different reset voltages. Reset predictions are unimodal for HRS and LRS and multimodal at intermediate voltages.

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Design and Implementation of Single-/Multi-Stage Small-Signal Amplifier Circuits Based on Locally Active Memristors

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As integrated circuit technology enters the post-Moore era, signal attenuation in interconnects has emerged as a critical bottleneck. Traditional repeater-based amplification schemes face severe challenges in terms of power consumption and spatial continuity. Owing to the negative differential resistance exhibited at specific bias points, locally active memristors provide a feasible approach for realizing novel signal amplification mechanisms. However, systematic circuit design methodologies and in-depth analyses of their amplification characteristics remain largely underdeveloped. This paper establishes a design framework for small-signal amplification circuits based on locally active memristors. First, frequency-domain modeling is employed to elucidate the physical mechanism of AC small-signal amplification. On this basis, a single-stage amplification circuit is designed, and the conditions for impedance matching and gain optimization are clarified. Furthermore, a multi-stage small-signal amplification circuit model was developed for a distributed coupling structure, and its stability as well as amplification performance under different bias conditions were systematically analyzed. The feasibility of the proposed designs is verified through both simulations and hardware experiments using the niobium oxide memristor and polynomial memristor. The results demonstrate the engineering potential of locally active memristors in analog signal processing, offering a novel theoretical foundation and technical pathway for the development of low-power, spatially continuous on-chip signal transmission systems.

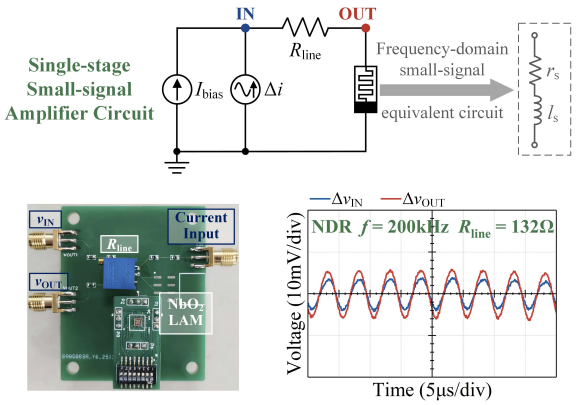


Figure 1. Schematic diagram and experimental results of single-stage small-signal amplifier circuit based on the NbO2 memritive device.

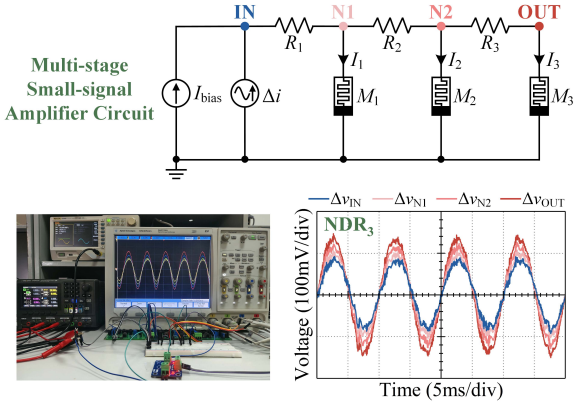


Figure 2. Schematic diagram and experimental results of multi-stage small-signal amplifier circuit based on the polynomial memristor.

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Talks

Neuro-inspired Computing

Anodic Memristors: From Electrochemical Oxide Growth to Tailored Resistive Switching Properties

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Anodic memristors are a class of resistive memory switching devices in which the active oxide layer is grown electrochemically from the bottom electrode instead of being deposited as a separate thin film. The parent materials used are valve metals, such as hafnium, niobium, tantalum, titanium, and tungsten, or their alloys. These metals readily form stable semiconducting or insulating oxides, making them suitable for resistive switching, non-volatile memory, neuromorphic computing, logic-in-memory and sensing applications. The main advantage of anodic memristors is namely the anodization process itself. It is a simple, low-cost and scalable method, which provides precise control over oxide thickness, composition and morphology. The oxide is formed directly from the underlying metal, which reduces fabrication complexity. Parameters such as anodization voltage, electrolyte composition, pH, scan rate and current density are able to modify the oxide growth rate, stoichiometry, structural uniformity and incorporated electrolyte species. This tunability makes anodic oxidation especially suitable for defect engineering, as memristive properties depend on oxygen vacancies, local non-stoichiometry, ionic mobility, charge trapping and electrode-oxide interfaces. By adjusting the anodization conditions, these defects can be introduced, redistributed or stabilized during oxide formation process itself. As a consequence, the switching voltage, electroforming criteria, resistance switching ratios, endurance, retention, volatility, and multilevel behavior can be tailored without complex post-treatments. The electrolyte used during anodization is crucial as its ions can be incorporated into the oxide and further influence conductivity, filament stability or interfacial barrier properties. Moreover, alloying valve metals can expand this control even further. Combinatorial thin-film libraries can be produced via co-sputtering two valve metals with a continuous compositional gradient across a single substrate. After anodization, the gradient becomes a mixed-oxide library containing many compositions prepared under identical conditions. Arrays of top electrodes then allow rapid, high-throughput electrical testing. This approach allows for rapid screening of composition-property relationships far more efficiently than the fabrication of separate alloys. In this way, monitoring minor compositional changes, which alter defect populations and switching behavior becomes possible [1]. For example, filamentary switching in Hf-Ta anodic memristors shows composition-dependent transitions between bipolar and unipolar behavior. Nanoscale HfO2 crystallites and elemental redistribution within the mixed oxide were linked to the enhanced performance, as seen in Fig. 1 (a) and (b) [1,2]. Furthermore, interfacial self-rectifying switching in the Nb-Ti system is illustrated in Fig. 2 (a),(b). Varying Ti concentrations produce homogeneous mixed anodic oxides without conductive filament formation. These devices show forming-free and volatile interfacial switching, in which oxygen-vacancy redistribution modulates the Schottky barrier. Their resistance changes, multilevel states and endurance up to one million cycles highlight how anodic defects and interface engineering can generate application-specific behavior [1,3]. Anodic memristors provide an accessible platform for rapidly designing, screening and optimizing functional oxide electronics with tailored end properties. Due to their versatility they can be implemented in self-rectifying crossbar devices, sensors and synaptic elements. These studies highlight the benefits of combinatorial research on anodic memristors in defect engineering, as well as their scalability and technological implementation in neuromorphic computing, memory technology and more [1].

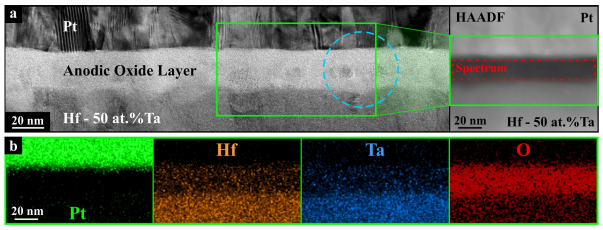


Figure 1. (a) Transmission electron microscopy image of a Hf-Ta anodic memristor showing small hafnium dioxide crystallites embedded in a mixed Hf-Ta anodic oxide as shown in (b) Scanning transmission electron microscopy with energy dispersive X-ray compositional maps of the region marked by a green frame,

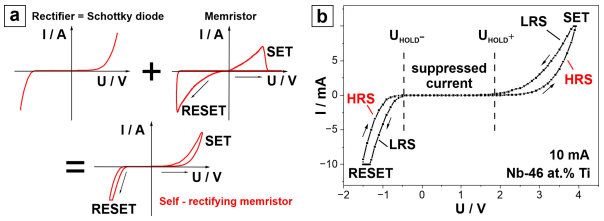


Figure 2. (a) A representation of typical I-U sweeps for a rectifier, a memristor and a self-rectifying memristor. (b) I-U sweep of a Nb- 46 at% Ti anodic memristor

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In-Operando Thermoreflectance Imaging of Heating Localization during Self-Oscillation in Vanadium Dioxide Nanowires Memristors.

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Neuromorphic hardware requires novel materials and engineering strategies to reduce computing power consumption [1]. Among envisaged solutions, vanadium-dioxide (VO_2)-based technologies have proven promising, from leaky-integrate-and-fire (LIF) neurons for spiking sensing [2] to biological-neuron emulation in a Hodgkin–Huxley (HH) configuration [3], and have recently been monolithically integrated with CMOS for energy-efficient spiking neurons [4]. Thanks to its near-room-temperature insulator-to-metal transition (IMT, ∼68 °C), a two-terminal VO_2 device exhibits volatile (threshold-switching) memristive behaviour [5]. The IMT is mainly driven by Joule heating, which initiates percolation of a metallic VO_2 conductive filament [6], the local response thus governs global device behaviour.

We study memristors patterned as five parallel nanowires (NWs) joined by a thin VO_2 carpet. The NWs are 100 nm wide, 200 nm thick, separated by 750 nm gaps bridged by a 60 nm-thick bottom carpet, with Cr/Au contacts (Fig. 1a). The devices show I–V stability across 50 cycles in both current- and voltage-driven operation at 40 °C (Fig. 1a). The negative differential resistance (NDR) range around 2.36 mA corresponds to a self-oscillating regime (Fig. 2a) averaged by the measurement unit: the device oscillates from ∼30 kHz at 1.9 mA to ∼50 kHz at 4.26 mA.

Local heat and current distributions are imaged by charge-coupled-device (CCD) thermoreflectance (TR) [7]. After calibration accounting for the NW-versus-carpet height difference, we performed steady-state TR. Once the IMT threshold current is exceeded, a localised metallic hot region appears. At 2 mA, within the NDR range, the mean heat stays confined and the steady-state temperature does not reach TIMT, with a channel maximum of ∼65 °C (Fig. 1b). At 5 mA the device is stable: heat spreads across it and peaks at the centre of the NW channel at ∼70 °C, above TIMT = 67 °C (Fig. 1c).

The transient domain (Fig. 2) clarifies these differences: temperature is sampled every 5 µs and averaged over 30 measurements for a 300 µs current pulse of 2 mA (Fig. 2a) or 5 mA (Fig. 2b). For 5 mA, after SMU stabilisation the temperature stays constant (69 °C) throughout; being Joule-driven, the phase change shows a 3.6 µs response time. At 2 mA, despite the constant current source, the VO_2 memristor's local activity generates voltage oscillations between VIMT and VMIT. The device repeatedly switches phase, and the temperature oscillates around TIMT, between 62 and 68 °C, explaining the mean 65 °C seen in steady state.

In conclusion, motivated by the potential of VO_2 NW memristors, we investigated their behaviour over their electro-thermal behaviour locally by thermoreflectance imaging. After establishing a methodology to map heat distribution at the NW scale, we showed that only a fraction of the device becomes conductive when switching from insulating to metallic state. This active region, studied dynamically, exhibits oscillating voltage and temperature under a 2 mA pulse in the NDR regime, whereas a 5 mA pulse yields constant voltage and temperature after a 3.6 µs response time. This clarifies the fundamental mechanisms of VO_2 NW memristors towards switching and neuromorphic architectures.

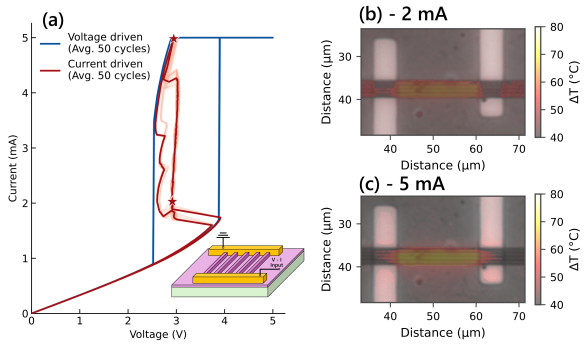


Figure 1. Electrical characterization and steady-state thermoreflectance (TR) measurement of a VO_2 NW-based memristor. (a) Fifty I–V curves in both current- and voltage-driven modes (individual cycles in light blue, averages shown as thick lines, chuck temperature fixed at 40 °C). Inset: schematic of the device under test (green = Si/SiO2 substrate, light purple = VO2 carpet, dark purple = VO2 NWs, yellow = Au contacts). (b–c) Temperature distribution in the device measured by steady-state TR at 2 mA (b) and 5 mA (c).

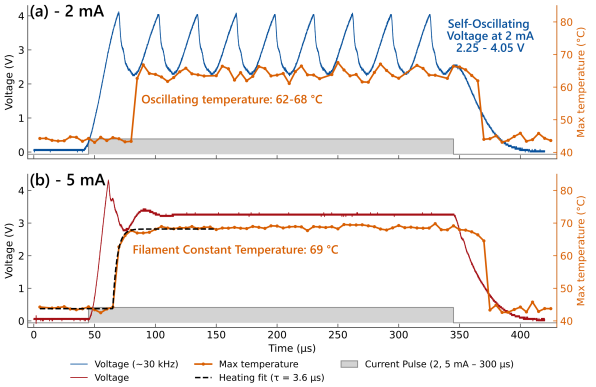


Figure 2. Transient study of the VO_2 NW-based memristor, showing the voltage response (blue/red) and the maximum temperature (orange) in the active channel in response to an input current pulse of 2 mA (a) or 5 mA (b).

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Machine Learning with Material Chaos

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Chaos is commonly observed in biological systems, from the bursting activity of individual neurons to the collective dynamics of neural networks. However, its potential for brain-inspired computing remains largely unexplored, raising the possibility that an alternative and more energy-efficient approach to computation may have been overlooked. In this work, we show that avalanche dynamics found in a range of material systems, including percolative filamentary networks, nanoparticle assemblies, and Barkhausen noise in two-dimensional ferroelectrics, originate from deterministic chaos with positive Lyapunov exponents ($\lambda > 0$). This provides a new way to understand a broad class of emergent material phenomena and highlights these systems as natural physical sources of chaotic dynamics.

Building on this observation, we use material-generated chaotic signals to realize the first hardware implementation of a Neurochaos Learning architecture. We demonstrate successful classification on tasks ranging from small datasets to the large-scale MNIST benchmark. Despite its simple architecture, the system achieves performance comparable to deep learning in low-data settings, performs better in continual-learning tasks by reducing catastrophic forgetting, and remains robust in the presence of noise. By showing that deterministic chaos is both an intrinsic property of memristive and ferroelectric materials and a useful computational resource, our work highlights the potential of chaos for neuromorphic computing and opens new possibilities for hardware-native intelligence.

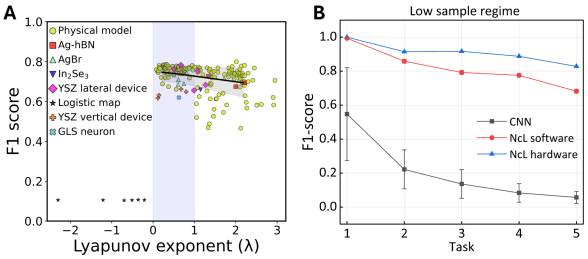


Figure 1. A. F1 vs Lyapunov exponent (λ) for different experimentally observed and physically modelled chaotic memristive systems and the mathematical GLS neuron and logistic map. B. Continual learning performance of a CNN, NcL algorithm, and hardware NcL with memristor chaotic trajectory in the low-sample regime (200 training and 500 test images).

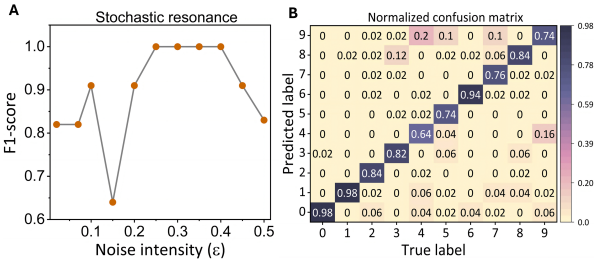


Figure 2. A. Stochastic resonance behavior obtained during hardware training on the Iris dataset. B. Normalized confusion matrix for MNIST handwritten dataset classification using (14x14) input images and 50 test samples/class (total 500 test samples).

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Gallium oxide barrier engineering in HZO ferroelectric tunnel junctions for analog synapses

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Ferroelectricity in HfO2-based thin films remains robust down to nanometer dimensions, and these materials are fully compatible with complementary metal oxide semiconductor (CMOS) processing. Hf0.5Zr0.5O2 (HZO) films can be crystallized into the polar orthorhombic phase at temperatures below 450 °C, making it back end of line (BEOL)compatible. Owing to their low-power operation, non-volatile data retention, and analog programmability, ferroelectric tunnel junctions (FTJs) have emerged as promising building blocks for next-generation neuromorphic computing. However, because scaling the HZO ferroelectric layer below 5 nm while retaining its ferroelectric properties is extremely challenging, bilayer FTJ architectures have been investigated, in which a 10 nm ferroelectric layer is combined with an ultrathin tunneling dielectric such as Al2O3 [1].

In this work, we investigated Hf0.5Zr0.5O2 (HZO)-based FTJs employing gallium oxide GaOx as the tunnel barrier (Fig. 1). Amorphous HZO (10 nm) and GaOx films were deposited at 250 °C by atomic layer deposition (ALD) and plasma-enhanced ALD (PEALD), respectively. Different thicknesses of GaOx were investigated (1.0, 1.5 and 2.0 nm). The oxygen vacancy content in GaOx was changed by varying the oxygen plasma dose times (3, 8, 10, and 30 s) [2]. After deposition, the stacks were annealed by rapid thermal processing (RTP) at 400 °C for 3 min in N_2 ambient, to crystallize HZO in the polar phase while GaOx remains amorphous.

We demonstrate high polarization values (Pr up to 20 μC/cm2), ON to OFF current ratio (I_ON/I_OFF) of 11 to 13 and synaptic functionalities. We will first discuss polarization and endurance as a function of the GaOx plasma dose time. We will then focus on the program erase endurance and synaptic functionality of the devices. We explored different pulse schemes (varying pulse amplitudes or pulse widths, constant pulses) to achieve gradual polarization switching and thus conductance modulation. In Fig. 2, we show program-erase endurance for four stacks (Pr ranges from 15 to $\sim$ 20 μC/cm2 for these stacks). The 30 and 10 s oxygen plasma dose time-based devices exhibit stable program erase endurance up to $10e^5$ cycles. Potentiation/depression measurements show that 16 stable conductance states are achieved. The increase in oxygen vacancy content (3 and 8 s plasma times) leads to fatigue occurring upon cycling and to low ON currents.

These results underscore the promise of GaOx as a tunnel barrier material for FTJ devices with a process that is fully BEOL compatible. Plasma-enhanced ALD allows for the control over the oxygen vacancy content in amorphous gallium oxide films, thereby providing a means to tailor the charge trap density within the tunneling barrier [3] to optimize the tunneling electroresistance (TER).

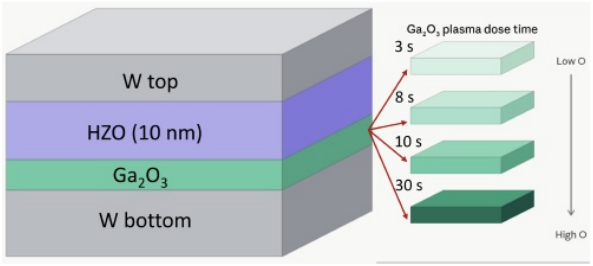


Figure 1. Sketch of the W/GaOx/HZO/W ferroelectric tunnel junction. The oxygen plasma dose time for the PEALD of GaOx was varied from 3 to 30 s.

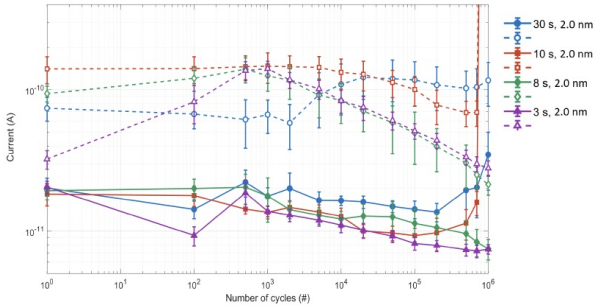


Figure 2. ON and OFF currents as a function of cycling for stacks with different GaOx (1 µs applied pulses - read pulse amplitude is 0.7 V and read time is 500 ms).

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Talks

Ising Machines

Towards Scalable High-Order Ising Machines and SAT Solvers with In-Memory Computing

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Many important problems in science and engineering, including cryptography, electronic design automation, electronic structure prediction, and logistics, can be formulated as discrete combinatorial optimization problems that are often NP-hard or NP-complete and remain computationally expensive on conventional computers. This has motivated the development of specialized hardware solvers called Ising machines that solve optimization problems by mapping them to the energy landscape of the Ising model [1]. However, existing approaches are limited in their ability to handle high-order cost functions. They either require hardware resources that scale exponentially with problem size [2], or rely on reducing problems to quadratic form, which degrades convergence time exponentially [3]. Consequently, solving large-scale high-order optimization problems remains a major limitation of existing hardware acceleration approaches. To address this, a new hardware paradigm that overcomes such exponential overheads is presented and its advantages are demonstrated through fabricated integrated circuits, tuned to solve small-scale high-order Boolean Satisfiability problems.

At the architectural level, a dual-crossbar compute-in-memory primitive is presented that enables discrete optimization problems to be mapped directly in high-order formulation, without requiring quadratization [4]. It enables massively parallel evaluation of high-order interactions and their associated gradients, a key operation in combinatorial search. By co-locating computation and storage, the design mitigates data-movement bottlenecks of conventional von Neumann architecture. This enables for the first time exponential improvements in both hardware-cost scaling and convergence-time scaling compared to existing approaches. Additional circuit and architectural techniques further extend the framework to support optimization problems directly in their native formulations, enabling general-purpose optimization accelerators without costly conversion to non-native representations and resulting in up to 3-4 orders improvement in convergence time. To enable scalability, a multi-tile architecture with programmable inter-tile communication is presented [5] that can support optimization problems with up to 100,000 variables in projected 28 nm CMOS implementations.

The proposed concepts are experimentally validated using two optimization chips fabricated in 55 nm CMOS technology. The first prototype integrates a SRAM-based dual-crossbar primitive with supporting circuitry for accelerating a legacy SAT-solving algorithm, demonstrating 1-2 orders improvement in speed over prior hardware solvers [6]. Furthermore, motivated by the inability of conventional SAT algorithms to fully exploit hardware parallelism, a new optimization algorithm co-designed for massively parallel architectures and achieving 10× improvement over prior methods is introduced. A second CMOS chip implementing this new algorithm incorporates probabilistic-bit circuits for massively parallel stochastic updates while eliminating high-precision ADCs, a major bottleneck in mixed-signal in-memory computing [7]. This chip represents the first silicon prototype capable of mapping arbitrary-order SAT problems while enabling parallel optimization dynamics. Despite using a legacy 55 nm CMOS node, it achieves up to 1,000× improvement over CPU and FPGA implementations, 40,000× improvement over quantum annealing hardware, and 3-100× improvement over prior integrated circuits in advanced technology nodes

Together, the experimentally demonstrated results and hardware-informed modeling establish a promising pathway toward large-scale high-order optimization accelerators that overcome the overheads of existing approaches and provide a viable classical pathway toward solving optimization problems with in-memory computing, often regarded as candidates for future quantum advantage.

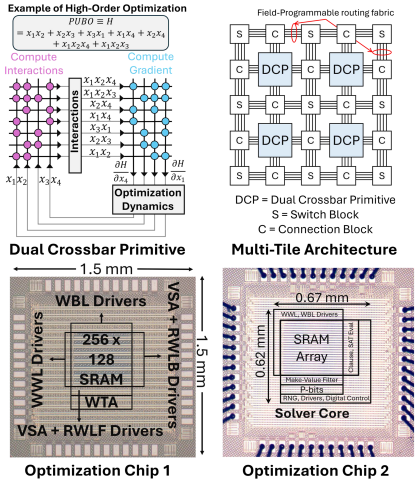
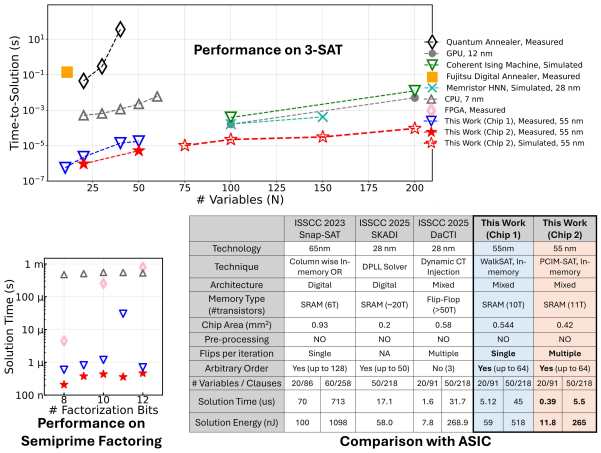


Figure 1. Overview of the dual crossbar primitive and multi-tile architecture, and micrographs of the two fabricated optimization chips.



	ISSCC 2023 Snap-SAT	ISSCC 2025 SKADI	ISSCC 2025 DaCTI	This Work (Chip 1)		This Work (Chip 2)	
Technology	65nm	28 nm	28 nm	55nm		55 nm	
Technique	Column wise In-memory OR	DPLL Solver	Dynamic CT Injection	WalkSAT, In-memory		PCIM-SAT, In-memory	
Architecture	Digital	Digital	Mixed	Mixed		Mixed	
Memory Type (#transistors)	SRAM (6T)	SRAM (~20T)	Flip-Flop (>50T)	SRAM (10T)		SRAM (11T)	
Chip Area (mm^2)	0.93	0.2	0.58	0.544		0.42	
Pre-processing	NO	NO	NO	NO		NO	
Flips per iteration	Single	NA	Multiple	**Single**		**Multiple**	
Arbitrary Order	Yes (up to 128)	Yes (up to 50)	No (3)	**Yes** (up to 64)		**Yes** (up to 64)	
# Variables / Clauses	20/86	60/258	50/218	20/91	50/218	20/91	50/218
Solution Time (us)	70	713	17.1	1.6	31.7	5.12	45	**0.39**	**5.5**
Solution Energy (nJ)	100	1098	58.0	7.8	268.9	59	518	**11.8**	**265**

Comparison with ASIC

Figure 2. Comparison of the chips' performance with other solvers on different representative optimization problems.

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Scalable RRAM-Based Analog Solver for Sparse Matrix Equations

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Large sparse linear systems underpin a broad range of computational workloads, including scientific computing, graph computing, and image super-resolution [1,2]. However, their structural irregularity leads to inefficient memory access on conventional digital processors and poor utilization when directly mapped onto dense RRAM crossbars. Sparse matrix-vector multiplication (MVM) accelerators can alleviate the mapping problem through partitioning, but still typically rely on discrete-time iterative algorithms, requiring repeated ADC/DAC transfers between analog arrays and digital control [3,4]. In contrast, closed-loop analog matrix inversion (INV) circuits can solve dense linear systems in continuous time, but partitioning strategies developed for sparse MVM are inapplicable to INV circuits, and effective INV-compatible partitioning methods remain lacking [5,6].

Here, we design a scalable INV-based analog sparse matrix equation solver using RRAM arrays. The solver reorganizes sparse matrices into hardware-compatible dense inversion tasks through block cyclic reduction, assisted by bandwidth-reducing reordering for irregular sparsity patterns [7]. The resulting dense sub-blocks are mapped onto Ta/HfO2/Pt 1T1R RRAM arrays and are solved by the analog matrix INV circuit, which solves the linear system of each matrix block in one step. To compensate for non-idealities and accumulated block-decomposition errors, we further develop a two-stage high-precision iteration strategy. Local high-precision MVM-based correction refines each block inversion result, while global high-precision refinement corrects the assembled sparse-system solution without re-executing the full reduction process.

We experimentally validate the proposed RRAM-based analog sparse matrix equation solver on two representative workloads. For diffusion-assisted image super-resolution, the inverse-convolution operation is accelerated by the proposed sparse solver, reconstructing a 64 x 64 low-resolution input into a 256 x 256 image with PSNR of 34.45 dB and SSIM of 0.905. For coupled microchannel flow-heat simulation, finite-volume discretization generates highly sparse Stokes and energy-equation systems; the two-stage high-precision iteration drives the residual below that obtained with SciPy spsolve. Benchmarking with a 64 x 64 analog block-inversion configuration indicates up to 341.38-fold runtime acceleration and 201.11-fold energy reduction. This work extends analog inversion from dense matrix primitives to scalable sparse linear-system solving, providing an algorithm-hardware co-design route for energy-efficient scientific, imaging, and other sparse linear algebra applications.

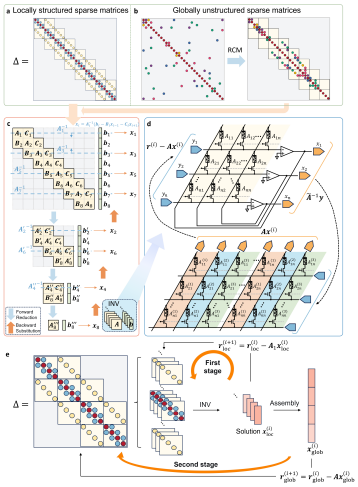


Figure 1. Hierarchical memristive analog inversion framework for sparse linear systems. Sparse matrices are reorganized into block-tridiagonal or bandwidth-reduced forms, decomposed by block cyclic reduction, and solved as dense block inversions using a closed-loop RRAM-OPA inversion circuit. Local and global residual refinement recover numerical precision from nonideal analog outputs.

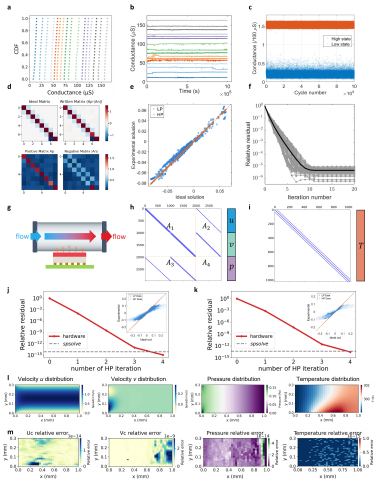


Figure 2. Experimental validation and sparse scientific-computing demonstration. RRAM-based analog inversion is validated by programmed matrix mapping and residual-corrected block solving. The solver is further demonstrated on coupled flow-heat partial differential equations, showing residual convergence to the double-precision regime, reconstructed velocity/pressure/temperature fields, and low relative errors versus digital sparse solvers.

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Solving QUBO Problems with Memristor-based Ising Machines

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A Quadratic Unconstrained Binary Optimization (QUBO) problem is a combinatorial optimization problem that involves finding the assignment of binary variables that minimizes or maximizes a certain objective function which has terms that are at most quadratic. Many classical problems from various fields, such as the Max-Cut problem shown in Fig. 1, can be formulated as QUBO problems. As these problems are typically NP-hard, it is not feasible to find an optimal solution by traditional digital computing, and efficient solvers are subject to considerable interest. One option is the so-called quantum annealer, that exploits quantum effects to find solutions. Another approach, that is implementable with classical electronics, is to transform the problem into an Ising model, which can be solved by a so-called Ising machine.

The Ising model can be implemented using coupled electrical oscillators stimulated at a particular frequency, where the phase of each oscillator represents the particle spin. However, current hardware implementations rely on coupling elements implemented in CMOS (e.g. op-amps) as shown in Fig. 2. As real-world problems require a dense connectivity, high area consumption of these coupling elements severely limits the scalability of current Ising machines.

The use of memristors addresses this difficulty: Compared to traditional SRAM-based memory cells, the 3D integration of memristive NV-memory using Back-End-Of-Line (BEOL) manufacturing significantly reduces the chip area needed. Our memristor-based Ising machines mainly target the coupling elements. In the first step, the conventional area and energy intensive biasing circuitry (DACs, internal memory and bias) is replaced with memristors. In the second step, memristors will be directly used as couplers.Memristors allow smaller coupling elements, more connections per oscillators and more spatial coupling without signal degradation, which is not possible in CMOS. This is an important step towards real-world usability. Another important aspect is the quality of the coupling, which is directly influenced by the accuracy of the couplers. Simulations have shown that at least 4 bit of resolution are required for the couplers, which is achievable with current memristor implementations.

With the successful tapeout and verification of a CMOS-based chip with 1440 oscillators in 28nm technology achieved previously at TU Darmstadt [1], we are currently preparing a Memristor-based (HfOx, Y2O3) implementation to replace the biasing circuitry in the context of the MesMerIsing project.

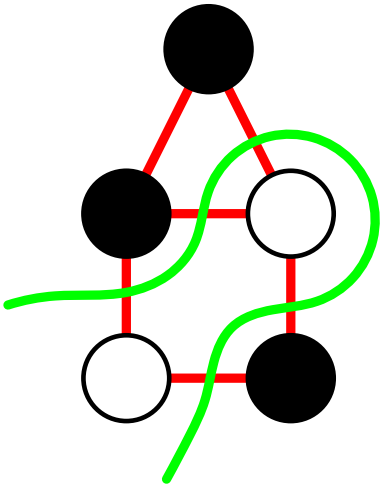


Figure 1. Example for a typical QUBO problem: Max-Cut

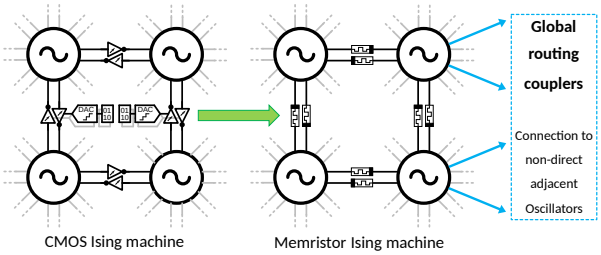


Figure 2. CMOS-based Ising machine and the equivalent memristor-based implementation with improved connectivity

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Closed-Loop In-Memory Computing for Energy-Based Nonlinear Optimization

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In-memory computing (IMC) has emerged as a powerful paradigm for accelerating linear algebra operations by tightly coupling memory and computation (Fig. 1a) [1]. Over the past decade, numerous demonstrations have shown that IMC can efficiently implement forward matrix–vector multiplication (MVM) [2]. More recently, a more advanced primitive for inverse matrix–vector multiplication (IMVM, Fig. 1b) has been experimentally demonstrated in a fully integrated test chip [3], enabling the acceleration of linear-system solvers with significant gains in latency and energy efficiency while offering promising prospects for large-scale integration.

Beyond linear algebra, recent results suggest that analog IMVM primitives can realize a much broader class of computational primitives. By exploiting closed-loop operation, such circuits naturally implement physical gradient-flow dynamics over an energy function defined by the programmed matrices, enabling the solution of problems that do not admit an explicit closed-form formulation (Fig. 1c) [4]. This observation shifts the role of IMC from that of a numerical linear solver to that of a hardware optimizer, where computation emerges from the physical evolution of the system toward an energy minimum. Furthermore, intrinsic and controllable nonlinearities of analog hardware, such as amplifier saturation, can be directly embedded within the physical dynamics, enabling constrained and nonlinear optimization without abandoning the energy-based computational framework [4,5].

Among the many application domains that could benefit from the energy efficiency of IMC, wireless communication systems provide a particularly compelling example. Modern 5G and emerging 6G networks rely on massive MIMO architectures, where signals transmitted by multiple users must be jointly processed at base stations under stringent latency, throughput, and power constraints [6]. The resulting uplink detection task can be formulated as a constrained nonlinear optimization problem, making it a natural target for closed-loop analog computing approaches.

However, despite substantial progress in both digital and analog accelerators, achieving high decoding accuracy without sacrificing energy efficiency remains a major challenge. Limited precision, hardware nonidealities, and nonlinear circuit behavior can significantly affect convergence and solution quality [7]. At the same time, unlike conventional linear-system solvers, MIMO detection requires the enforcement of discrete symbol constraints, introducing a fundamentally nonlinear optimization landscape. Recent work has shown that these challenges can be addressed by engineering closed-loop IMC architectures whose physical dynamics directly incorporate the required nonlinear constraints. By combining analog energy minimization with lightweight digital iterative-refinement techniques, it becomes possible to achieve solution accuracies significantly exceeding the intrinsic precision of the underlying analog hardware, while preserving its energy-efficiency advantages and meeting the accuracy requirements of practical communication systems.

This talk presents recent advances along this trajectory, including a high-precision nonlinear physical solver for massive MIMO detection based on coupled closed-loop analog IMC circuits and digital iterative refinement. More broadly, it illustrates how closed-loop IMC can evolve from a linear-algebra accelerator into a general-purpose high-precision physical computing framework, opening a path toward scalable hardware acceleration of nonlinear inverse problems and, more broadly, energy-based physical computing.

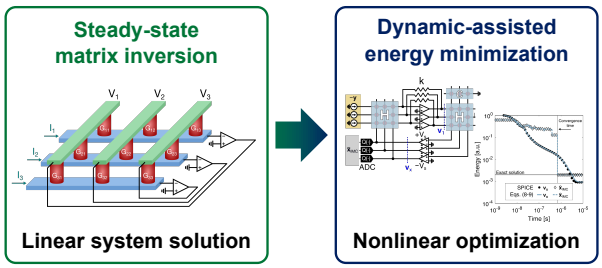


Figure 1. Evolution of closed-loop IMC from steady-state matrix inversion for linear-system solution (left) to dynamic-assisted energy minimization for nonlinear optimization (right).

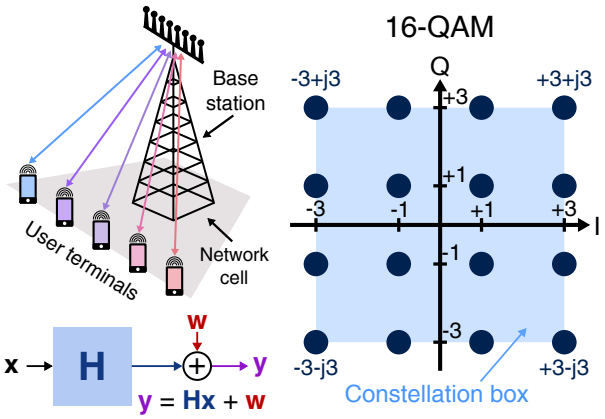


Figure 2. Massive MIMO detection. Multiple user transmissions are mixed by the wireless channel matrix H and corrupted by noise, yielding the received signal y = Hx + w. Decoding the transmitted symbols requires solving a constrained nonlinear inverse problem, where the solution must belong to a discrete modulation constellation (16-QAM shown).

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Talks

High Frequency / Ultrafast / Devices

Design and Performance Analysis of RF Switches Based on Resistive Switching Devices

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The increasing demand for reconfigurable and energy-efficient wireless communication systems for beyond-5G and 6G applications has intensified research into compact, low-power, and high-linearity RF switching technologies. Conventional RF switches based on CMOS and MEMS technologies often face trade-offs between insertion loss, isolation, switching speed, reliability, fabrication complexity, and power consumption. In this context, resistive switching devices have emerged as promising candidates for next-generation RF switching platforms due to their non-volatile behavior, ultra-low static power consumption, scalability, and compatibility with emerging nanomaterials.

This invited talk presents the design principles, fabrication approaches, and RF performance analysis of resistive switching devices, with particular emphasis on MoS2-based switching structures. A brief overview of the state-of-the-art in resistive switching RF switches will be discussed, covering conductive-bridge RAM (CBRAM), oxide-based memristive devices, phase-change materials, and two-dimensional material platforms for microwave and reconfigurable intelligent surface (RIS) applications. Key RF metrics including insertion loss, isolation, switching endurance, ON/OFF resistance ratio, and frequency scalability will be reviewed in comparison with conventional RF technologies.

The presentation will focus on our recent experimental results obtained from MoS2 resistive switching devices fabricated using a liquid–liquid interface synthesis method. The liquid–liquid interface approach enables controlled growth of thin MoS2 layers with improved uniformity and scalable processing. Electrical and RF characterization results demonstrate stable resistive switching behavior suitable for RF switching operation, with promising impedance reconfigurability and low-power switching characteristics.

Finally, the talk will discuss the integration potential of resistive switching devices in reconfigurable intelligent surfaces (RIS), tunable RF front ends, and adaptive wireless communication systems. The presented results highlight the potential of MoS2-based resistive switching technology as a viable pathway toward compact, energy-efficient, and highly reconfigurable RF hardware for future communication networks.

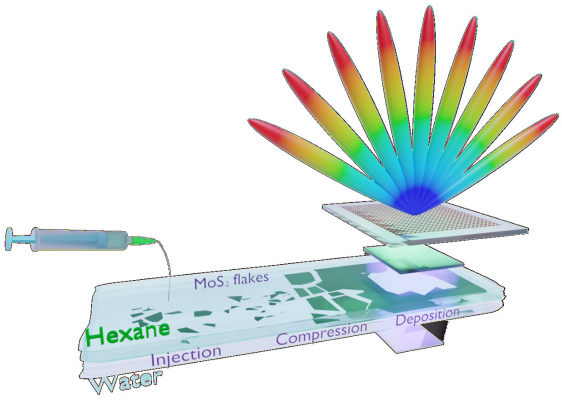


Figure 1. 2D Memristor RF Switches for Scalable Reconfigurable Intelligent Surfaces at D-Band

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Toward GHz operation of oscillating neural networks

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Phase-encoded oscillating neural networks (ONNs) realized with capacitively coupled simple circuits of Mott memristors have been demonstrated recently to solve complex optimization problems such as graph-coloring and max-cut [1]. In essence, the problem is encoded in the couplings of the oscillator network. The solution, worked out exclusively by the physics of the neural network hardware, is represented in the synchronized phases of the oscillators. To exploit the full potential in operation speed and energy-efficiency of such ONNs, in our recent work we have explored the pathways to optimize the device layout and circuit environment of the VO2 Mott memristors. As a result, the operating frequency was increased from the MHz range to 167 MHz [2], using devices whose active area was limited by the resolution of e-beam lithography. Here, we present an electromigration-based patterning technique that further reduces the active area to truly nanometer dimensions at low cost and high yield. This, combined with the on-chip integration of the oscillator circuits, facilitates stable oscillations up to 0.64 GHz, approaching the clock frequencies of conventional computing while also enabling energy efficient operation down to 1 pJ / oscillation.

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Tri-Functional Oxide Nanoelectronic devices for Neuromorphic Hardware

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The continued scaling of complementary metal–oxide–semiconductor (CMOS) technology is approaching fundamental physical limits, while the separation of memory and processing units in conventional computing architectures results in significant energy and speed bottlenecks. Reconfigurable electronic devices capable of performing multiple functionalities within a single structure offer a promising route toward reducing circuit complexity, footprint, and power consumption. In parallel, brain-inspired computing architectures based on artificial neural networks have emerged as attractive solutions for energy-efficient information processing.Here, we demonstrate a multifunctional oxide interface-based nanowire device in which transistor, memristive, and memcapacitive functionalities can be dynamically reconfigured through electrical biasing (see Fig. 1). The device exploits the quasi-two-dimensional electron system formed at $LaAlO_3/SrTiO_3$ heterointerfaces, enabling a versatile platform for neuromorphic and logic-in-memory applications [1]. In the transistor–memcapacitor configuration, the device exhibits nonlinear dynamics and short-term memory characteristics, enabling its implementation as a physical reservoir computing system as schematically shown in Fig. 2. Using a simple 4-bit pulse encoding scheme, we demonstrate pattern-recognition capability with fast read–write operation. In the transistor–memristor configuration, the device mimics synaptic behavior, exhibiting both short- and long-term plasticity, including learning, forgetting, and nonvolatile memory functionalities. Furthermore, logic-in-memory operations are realized in a two-transistor–one-memristor architecture, where OR and AND logic functions are performed together with in-situ storage of the logic output by exploiting the memristor's long-term memory. Remarkably, the same device structure can be electrically reconfigured between OR and AND synaptic logic operations, highlighting its potential for adaptive decision-making applications, such as intelligent healthcare monitoring systems.The integration of reservoir computing, logic-in-memory, synaptic functionality, and runtime reconfigurability within a single oxide nanostructure establishes a pathway toward monolithically integrated, energy-efficient, and adaptive neuromorphic hardware [2]. These findings position oxide nanostructures as a promising platform for beyond-CMOS computing architectures.

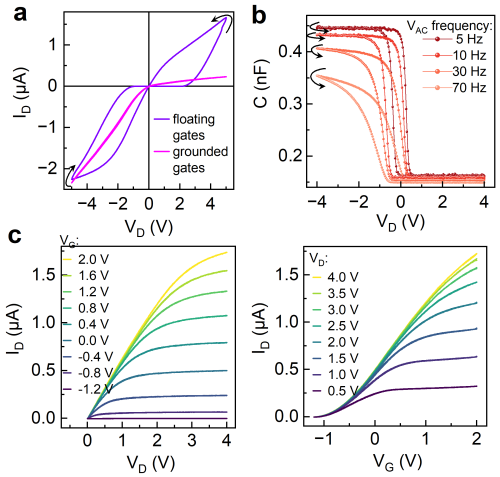


Figure 1. (a) memristive, (b) memcapacitive and (c) transistor characteristics of $LaAlO_3/SrTiO_3$-based lateral nanoelectronic device.

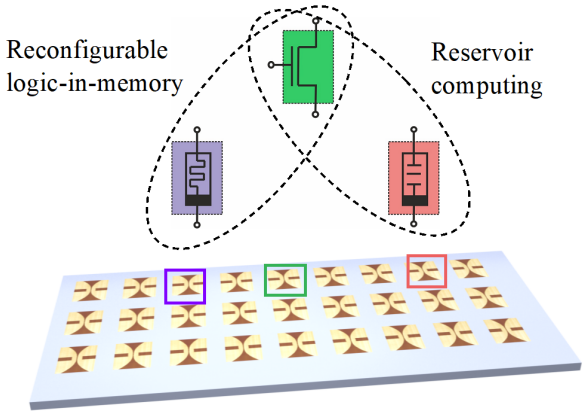


Figure 2. Schematic illustration showing reservoir computing applications integrating transistor-memcapacitor devices and reconfigurable logic-in-memory applications in a transistor-memristor integrated circuit on the same platform.

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Evaluating HfO_2-based RRAM at Cryogenic Temperatures for Reliable Cryo-Compatible Memory Applications

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Quantum computers operate at millikelvin temperatures, and scaling them requires moving the control electronics close to the qubits using cryogenic CMOS. The memory supporting this cryogenic logic remains the least mature component of the cold stack [1]. Resistive random-access memory (RRAM) has emerged as a promising candidate as cryogenic-compatible memory owing to its non-volatile nature, multi-level cell (MLC), and ability to operate at extreme conditions such as cryogenic temperatures [2,3]. Yet a complete performance evaluation below 4 K is still missing, which this work addresses.

We present the first systematic study of HfO_2-based RRAM operation at 1.5 K on 1-transistor-1-resistor (1T1R) arrays fabricated in IHP's 130 nm BiCMOS technology (Fig. 1a). Each cell integrates a nMOS transistor as selector device, with dimensions W = 8 µm and L = 0.66 µm. The RRAM device is a BEOL-integrated TiN/Al:HfO_2/Ti/TiN metal-insulator-metal (MIM) stack. The HfO_2 layer is doped with 5% Al to improve the resistive switching yield [4]. The test array follows a 9×4 topology, with standalone transistors placed in the ninth row to enable independent characterization of the selector.

In the initial test, 15 RRAM devices were formed at 300 K and 1.5 K (Fig. 1b) and programmed at 1.5 K into four levels, three low-resistance states (LRSs) and one high-resistance state (HRS) following the procedure in [3] (Fig. 1c and d), and 1000 endurance cycles were carried out at the lowest temperature. The results revealed device failures and stuck-at-LRS at cryogenic temperatures. To address this, we analyzed the nMOS output and transfer characteristics at cryogenic temperature to develop an optimized programming scheme to prevent over-programming of the RRAM cells at 1.5 K.

Guided by these insights, a second batch of 15 RRAM devices were formed and programmed at 300 K into six optimized MLC levels (five LRSs and one HRS) (Fig. 1e), and reliability was then assessed at 1.5 K including endurance and read-disturbance tests (Fig. 2). The level targets were chosen by evaluating the output and transfer characteristics of the nMOS selector from 300 K down to 1.5 K.The resistance distribution of each level across 1000 endurance cycles (Fig. 2a), represented as a probability density function (PDF) and fitted with a Gaussian distribution, confirmed that the five LRS levels remained ordered and well separated even at the lowest temperature. The more resistive LRS distributions showed a downward shift, attributed to weaker filament formation, while the HRS distributions (Fig. 2b) showed an upward shift toward higher current levels, due to incomplete filament rupture [3]. Fig. 2c presents the read-disturbance results over 1000 consecutive readouts performed at 0.2 V for all programmed levels. The median and standard deviation indicate stable readout currents even after continuous stress, with the lower-conductance levels showing slightly larger fluctuations, consistent with weaker filaments. These results demonstrate that the 1T1R RRAM devices can support stable multi-level operation at 1.5 K when the selector transistor compliance is optimized, making them suitable for cryogenic and quantum computing applications.

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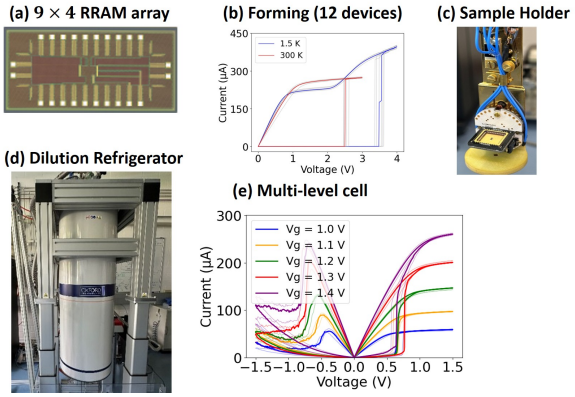


Figure 1. Cryogenic setup and multi-level switching of the Al:HfO_2 1T1R RRAM (a) 9×4 1T1R array in IHP's 130 nm BiCMOS technology and (b) Forming I-V at 1.5 K and 300 K. (c) chip mounted on the cold stage sample holder. (d) Dilution refrigerator. (e) MLC operation at 300 K showing five resistance levels set by gate voltage (Vg= 1.0 V-1.4 V), faint lines are per device median, bold lines are across device median.

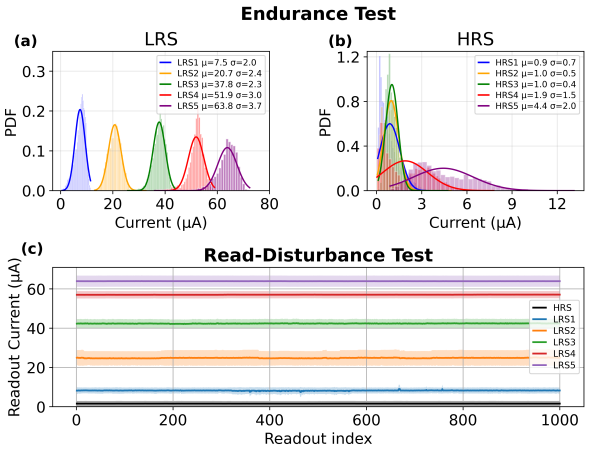


Figure 2. Endurance and read-disturbance characteristics of the HfO_2-based RRAM array over 1000 cycles at 1.5 K of 3 devices in each level. (a) Gaussian-fitted current PDF for five LRS levels (LRS1-LRS 5). (b) Gaussian-fitted current PDF for the five HRS levels (HRS1-HRS5). (c) Mean readout current and standard deviation versus readout index for HRS and LRS state, showing read disturbance stability.

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Talks

Synaptic Behavior

Time-series prediction with compact memristor circuits over a wide, adjustable operating frequency range

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Energy efficiency and computational speed are among the most critical parameters in neuromorphic computing. Traditional approaches focus on translating neural networks into more efficient hardware implementations, where individual elements are simple but the interconnecting networks are highly complex. An alternative approach replaces network complexity with dynamic complexity; that is, the input data is first pre-processed by a dynamic reservoir layer, whose responses are aggregated into output values by a simple readout layer. However, most hardware-based reservoir computing solutions rely on a "black box"-like operation with little insight into the operational dynamics. Memristive devices offer an excellent balance between complexity, traceability and controllability: thanks to their highly voltage-dependent switching speeds, they possess excellent dynamic properties for reservoir computing applications, while the operation of individual elements remains sufficiently understandable.

Here, we utilize the dynamic properties of non-volatile memristive devices for efficient time-series prediction. To this end, we apply a novel information processing scheme [1], where the incoming information is delivered to the system in the form of positive pulses of varying amplitude, while the subsequent negative offset pulses enable an adjustable forgetting mechanism that can be used to fine-tune shorter or longer term memory functionalities. When testing this framework on benchmark time series prediction problems, we find that, thanks to the tunability of the forgetting dynamics, very high prediction accuracy can be achieved using a surprisingly small number of memristive input channels. Furthermore, this scheme allows for the tunability of the operating frequency over many orders of magnitude. We demonstrate that by simply adjusting the input voltage levels, the information processing speed of the same memristive dynamic layer can be increased from the kHz to the MHz range while maintaining excellent prediction accuracy.

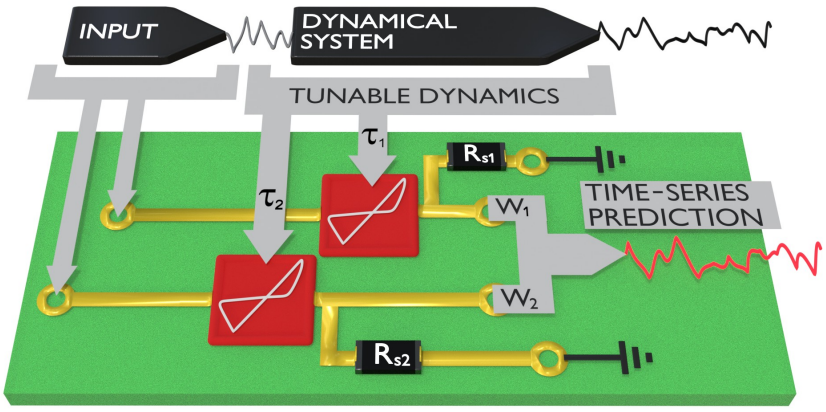


Figure 1. Efficient time-series prediction with only two dynamical memristors

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Time-Dependent Synaptic Plasticity and Neuromorphic Potential of Ag-Doped VCeOx-Based Analog RRAM Devices

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Although mobile metal-ion-based filamentary memristors have been extensively investigated as artificial synapses for neuromorphic computing architectures, their practical implementation is fundamentally constrained by stochastic growth and abrupt switching dynamics. To overcome these critical limitations, this study demonstrates a high-performance non-filamentary synaptic memristor based on mobile silver-doped vanadium-cerium oxide with Pt/VCeOx:Ag/Pt structure (Fig. 1). The proposed device achieves exceptionally linear and symmetric conductance modulation with robust endurance spanning over 1E4 consecutive potentiation and depression cycles. This outstanding performance originates from a hybrid conduction mechanism that synergistically combines the localized effects of embedded Ag nanoclusters with the controlled redistribution of mobile Ag ions under an electric field (Fig. 1). This conjugated contribution enables highly reliable, polarity-dependent, and reproducible analog switching behaviors, which are essential for precise synaptic weight updates. Comprehensive material and electrical characterizations were conducted to elucidate the underlying physics; transmission electron microscopy (TEM) analysis successfully confirms the uniform presence of Ag nanoclusters (data not shown), while Kelvin probe force microscopy (KPFM) explicitly verifies the field-driven migration and spatial redistribution of residual Ag ions within the oxide matrix (Fig. 2). Furthermore, vital time-dependent synaptic plasticity functions, which includes paired-pulse facilitation (PPF), post-tetanic potentiation (PTP), spike-rate-dependent plasticity (SRDP), and the critical transition from short-term memory to long-term memory (STM-to-LTM), were comprehensively characterized (Fig. 2). Harnessing these intrinsic temporal dynamics, we successfully implemented a hardware-backed reservoir computing (RC) system. The VCeOx:Ag-based RC framework achieves high classification accuracies of 90.6% and 76.7% for the handwritten digit-MNIST and Fashion-MNIST datasets, respectively, validating its capability for advanced spatio-temporal pattern recognition (Fig. 2). These findings underscore that the VCeOx:Ag memristor, governed by a complementary and synergistic switching mechanism, offers unprecedented control over analog conductance states. Consequently, this work paves a promising alternative pathway for developing highly scalable, hardware-secure, and energy-efficient neuromorphic computing systems tailored for edge artificial intelligence (AI) and decentralized on-device learning applications.

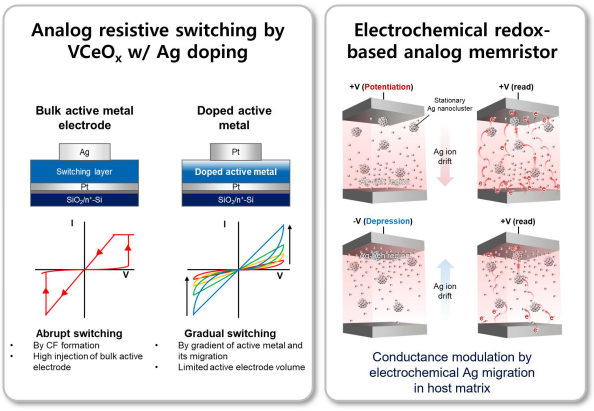


Figure 1. Device optimization strategies for implementing robust analog weight update by doping mobile metal species.

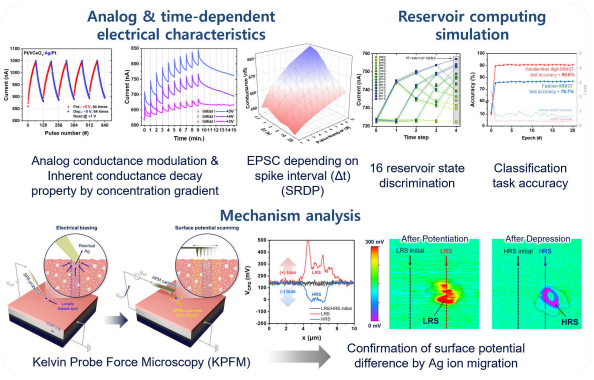


Figure 2. Time-dependent synaptic characteristics of Pt/VCeOx:Ag/Pt memristor and its application in a reservoir computing (RC) framework for spatio-temporal data processing (above). Confirmation of surface potential difference by Ag ion migration through KPFM analysis (below).

Multimodal Learning and Dual-Wavelength Information Encoding in CuPc-Based Optoelectronic Artificial Synapses

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The increasing demand for energy-efficient and intelligent computing has driven the development of neuromorphic devices that emulate the adaptive learning capability of the human brain. Optoelectronic neuromorphic systems are particularly attractive because they integrate sensing, memory, and processing within a single platform. Among the various material systems explored, organic semiconductors offer unique advantages due to their tunable optoelectronic properties, low-cost fabrication, and strong interaction with light.

In this work, we demonstrate an optoelectronic artificial synapse based on an ITO/CuPc/Al heterostructure. Owing to the strong visible-light absorption of Copper Phthalocyanine (CuPc), especially in the red spectral region, the device exhibits pronounced responses to both electrical and optical stimuli. The device successfully emulates key synaptic functions, including paired-pulse facilitation, spike-number-dependent plasticity, and long-term memory behavior, highlighting its capability for multimodal information processing.

The device further demonstrates associative learning between light and voltage stimuli through the realization of Pavlovian conditioning. By repeatedly pairing optical and electrical inputs, a learned association is established, enabling enhanced synaptic responses. This property is subsequently utilized to improve pattern recognition accuracy through optical assistance.

In addition, the wavelength-dependent photoresponse of the device is exploited for dual-wavelength information encoding. Distinct responses to red and blue illumination are employed to implement Morse code-based optical encoding, demonstrating the potential of the device for secure optical communication and cryptographic applications.

The coexistence of multimodal synaptic plasticity, associative learning, optically enhanced pattern recognition, and wavelength-selective information encoding establishes the ITO/CuPc/Al device as a versatile platform for next-generation neuromorphic computing, artificial vision, and intelligent optical information processing.

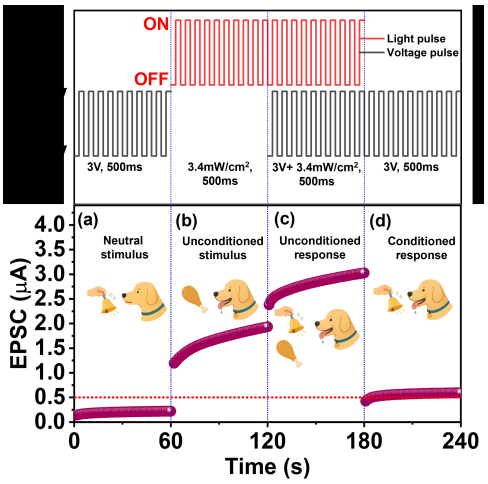


Figure 1. Demonstration of Pavlov Dog theory, showing the transfer of voltage pulses as a conditioned stimulus after the conditioning process, inducing a response.

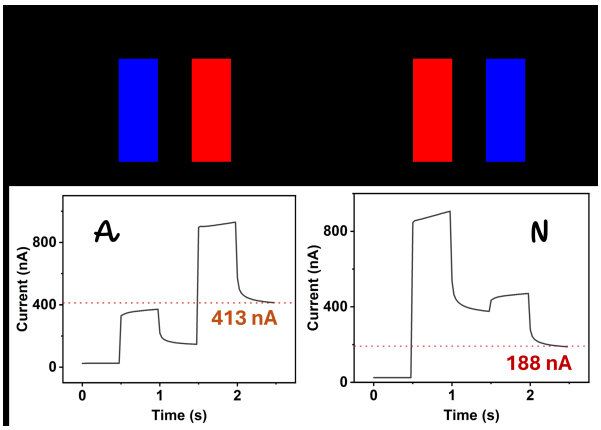


Figure 2. Dual-wavelength Morse code encoding showing temporal feature extraction, where identical optical pulses arranged in different temporal sequences ("A" and "N") produce distinct conductance states (413 and 188 nA).

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Unraveling the Local Current-Limit Mechanism behind Linear, Low-Voltage Synaptic Update in IGZO/Cu:Te Bilayer Memristors

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Analog memristive synapses for energy-efficient neuromorphic computing require a conductance that updates linearly and symmetrically under identical voltage pulses, yet filamentary devices typically switch abruptly because filament growth is governed by self-accelerating positive feedback. Here we show that interface engineering — inserting a high-resistance IGZO layer in series with a Cu:Te electrochemical-metallization switching layer — simultaneously linearizes the long-term potentiation/depression (LTP/LTD) update and lowers the pulse operating voltage, without altering the quasi-static DC characteristics. Three devices with progressively higher top-layer resistivity — LR (single layer), LR/MR, and LR/HR — were fabricated and compared. As the IGZO resistance increases, the update nonlinearity falls from ∼0.9 to ∼0.1 and the pulse operating voltage drops from 2.2 to 1.2 V, while the DC sweeps and the measured layer thermal conductivities remain essentially identical, ruling out differing self-heating as the cause.

In order to identify the mechanism, a measurement-anchored local-resistor multi-filament model was developed. In this model, each nanoscale filament is current-limited by its own local IGZO column, rather than by a shared global resistor. The framework under scrutiny herein reproduces the full device history. This is achieved by means of a common ∼2 V forming sweep with a self-limited (<1 mA) current. This current is divided by the per-filament current, with the result that only a fraction (φ = 2/8/40% of a shared 100-site nucleation pool; N = 2/8/40 filaments for LR/LR/MR/LR/HR) is activated. This is followed by the subsequent pulsed LTP/LTD response, which is emulated under 250 + 250 identical 250 ns pulses. These pulses match the measured curve shapes and conductance window (dynamic range ≈ 4–9). The unifying picture is that the series resistance caps the current any single filament can draw, thereby suppressing the winner-takes-all runaway and redistributing the current budget into many weak filaments. This results in a filament gap that is confined to a narrow window, and a forward decomposition V_op = V_gap + I·R_s demonstrates that the collapse of the gap re-bridging field (V_gap, gap shrinking from 1.55 to 0.28 nm) dominates the modest growth of the series IR term. Consequently, the highest-resistance device paradoxically operates at the lowest voltage. The local, per-column nature of the limitation, set by geometry rather than resistivity, is pivotal in converting interface tuning into linear, symmetric, low-voltage synaptic behaviour. Finally, the linearized devices were applied as synaptic weights in a spiking neural network (SNN), where the enhanced linearity and symmetry yielded high recognition accuracy on the MNIST database, thus confirming the system-level benefit of interface engineering.

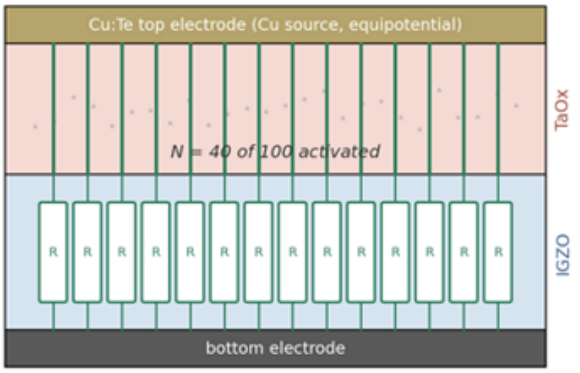


Figure 1. Local current-limit model: Cu filaments in TaOx, each limited by its own underlying IGZO column resistance.

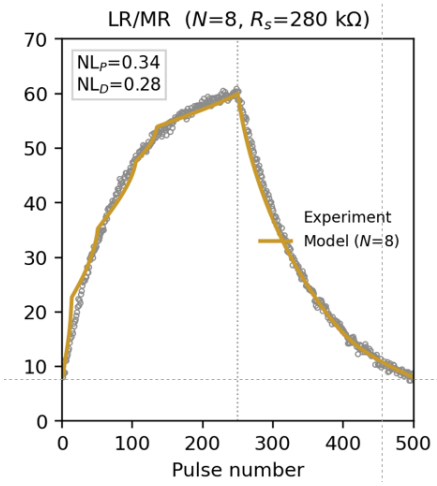


Figure 2. Experiment (open circles) vs. multi-filament simulation (solid line) for the TaOx/CuTe device, with the model trace affine-mapped onto the measured conductance window.

Talks

Crossbar Arrays

The case of ferroelectric memristors and memcapacitors in passive crossbar arrays

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Ferroelectric memristors are 2-terminal non-volatile memory devices that - in contrast to most other resistive switches - can be switched through the application of an electrical field, rather than forcing a current through the devices. Thus, the switching process does not involve joule heating, giving rise to a very energy efficient switching mechanism. The current modulation is based on a polarization-dependent transport mechanism, that is typically attained by utilization of semi-conducting electrodes [1] or by insertion of an additional dielectric material layer between one electrode and the ferroelectric that acts as a tunneling layer [2]. First ferroelectric tunneling junctions (FTJ) utilizing ferroelectric HfO2 have been already reported back in 2016 [3] and since then have been subject of intensifying research.

Due to their asymmetric stack configuration that leads to a rectifying behavior FTJs are interesting candidates for utilization in scalable selector-less passive cross-bar arrays. The typically very small read-currents in the pA-range bear challenges for their adoption in pure memory arrays. However, this high-impedance feature, which helps avoiding the occurrence of significant voltage drop along the word- and bit-lines, is very interesting when targeting for the parallel readout of a huge number of FTJs, e.g. performing analogue vector-matrix-multiplication (VMM) [4]. Thus, FTJs are considered as extremely energy efficient resistive switches being suitable for massive parallel operation and analogue in-memory computing (IMC).

Moreover, while application of an electrical field larger than the coercive field of the ferroelectric layer causes state-altering polarization switching, the application of an electric field that is slightly lower than the coercive field causes progressively reorientation of ferroelectric dipoles. This in turn induced a shift of the energy minima in the Landau energy landscape being origin of multiple capacitive states [5]. Thus, in addition to the memristive properties, FTJs (similar as pure ferroelectric capacitors) exhibit memcapacitive features that can be used for non-destructive readout as well.

In this work we discuss the specific electrical properties of ferroelectric/dielectric double-layer FTJs with respect to their memristive and memcapacitive behaviour. Fig. 1 depicts the measured current response of a 25µm^2 FTJ to a triangular voltage signal (inset). The IV-characteristic shows the self-rectified dc-tunneling current Idc, the capacitive displacement current Idisp, and polarization current Ipol. The shaded area depicts the readout region for either memristive or memcapacitive readout. The electrical switching kinetics for state update, the readout mechanisms and their impact on selector-less array operation are investigated. Finally, first results of the hardware implementation of a 32x32 FTJ crossbar array that is integrated in the BEOL of a CMOS chip including a serial addressing scheme as well as an on-chip sensing circuit (Fig. 2) are shared. Our findings give guidance for proper device operation as well as future device and circuit optimization.

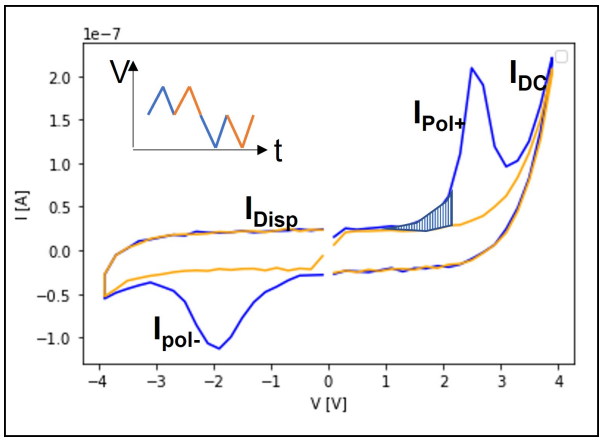


Figure 1. FTJ current response to a triangular voltage signal, the shaded area indicating the suitable region for both - memristive and memcapacitive readout operation.

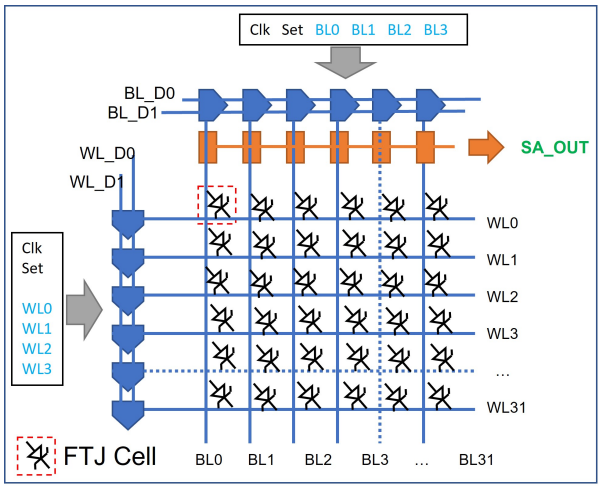


Figure 2. Schematic representation of a 32x32 FTJ crossbar array, integrated into the BEOL of a CMOS chip

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Application of Memristors for Implementation of a Modified Hebbian Learning Rule

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The Hebbian learning rule is one of the most common and basic learning methods used in unsupervised neural networks[1]. Although widely used in neural networks, scholars continue to seek to refine the learning rule to optimize performance [2-8]. In this talk, we discuss how the traditional Hebbian learning rule, along with other attempts to improve it, fails to fully capture the relationship between synaptic weight changes and the activity voltages in two neurons. An

improved Hebbian learning rule that addresses this shortcoming is introduced. Specifically, the following synaptic weight update rule is used:

$$W_{i,j}(n+1)=W_{i,j}(n)+1/2\ \alpha(x_i x_j-1)+[1/4\ \beta(x_i+1)(x_j+1)-1/4\ \gamma(x_i-1)(x_j-1)]$$

where W represents the synaptic weight, xi,xj represent normalized neuron activity, either +1 or -1, whereas α, β, and γ are positive constants that account for learning and forgetting rates.

Extensive circuit simulation was performed using LTspice and the HP memristor model. The simulation results demonstrate the efficacy of the modified rule and the biopausible functionality of the memristor-based Pavlov associative memory circuit.

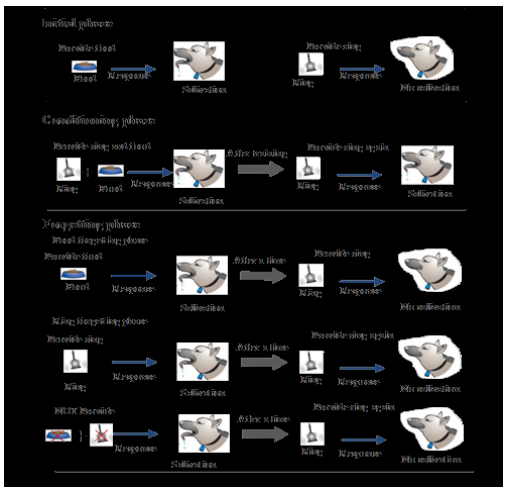


Figure 1. The process of Pavlov's associative memory experiment with Application of Memristors for Implementation of the modified hebbian learning Rule

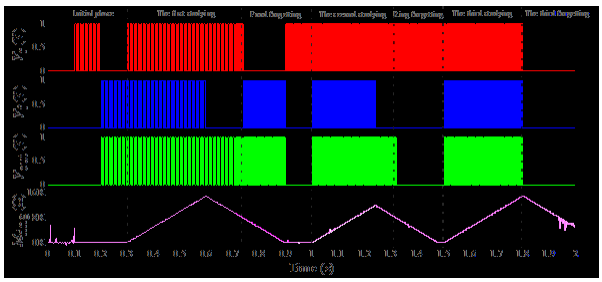


Figure 2. Simulation result of Pavlov associative memory circuit based on the modified hebbian learning rule

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Impact of variations in n-type MOSFET electrical characteristics on 1T1R RRAM cells performance

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RRAM technology is well known because of its validated performance in terms of low-voltage programming, CMOS compatibility, high scalability, and long endurance and data retention [1]. However, this technology is also well known because of its inherent variability [2]. Both device-to-device (D2D) and cycle-to-cycle (C2C) variabilities can be reduced, but not completely removed. One of the most reliable architectures for integrating RRAM cells is the so-called 1-transistor-1-resistor (1T1R), which places a MOSFET transistor in series with the RRAM device in order to provide current control during Forming and Set operations. In particular, this configuration is of high interest in the Multi-Level Cell (MLC) approach [3]. Since the variability of the RRAM device itself is already well proved, the study of variability within 1T1R RRAM cells just focuses on the RRAM electrical characteristics. However, although it is lower, the variability emerging from the transistor cannot be neglected. In this work, the impact of variations in the electrical characteristics of the n-type MOSTET (nMOS) integrated within the 1T1R cell on the RRAM performance (Forming, Reset and Set operations) are analyzed in detail.

The samples used for this study were fabricated in the CMOS 130 nm technology at IHP. The RRAM devices consist of the following metal-insulator-metal (MIM) stack: TiN/Al:HfO2/Ti/TiN. Different sources of variation in the electrical characteristics of the nMOS are considered, such as, nMOS dimensions with widths (W) equal to 150, 500, 1000 and 4000 nm, nMOS D2D variability across 61 devices over a 200 mm wafer, and temperatures ranging from -40 to 150 °C.

As shown in Fig. 1 for the nMOS with W = 1000 nm, the output IV characteristic of 61 nMOS with Vg = 1.2 V (black lines) presents obvious D2D variations. These variations influence the Forming operation of the corresponding RRAM cell (green lines), where the nMOS plays a fundamental role in limiting the current flowing through the RRAM device. In Fig. 2, it can be seen how this nMOS IV variability during Forming partially shapes the variability of the conductance state programmed for all nMOS sizes.

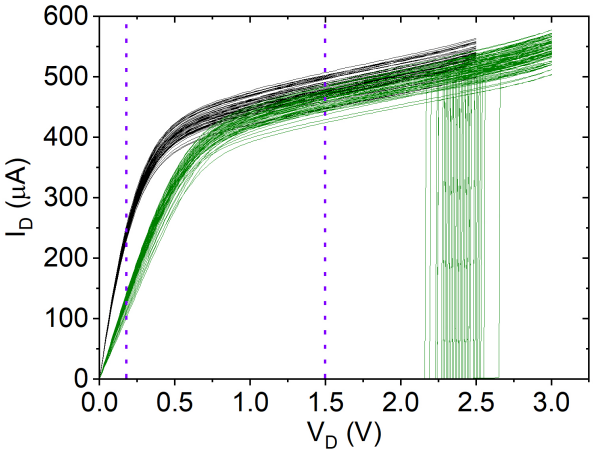


Figure 1. IV characteristics of 61 nMOS devices with W = 1000 nm at Vg = 1.2 V (black lines) and the corresponding IV characteristics measured during Forming (green lines).

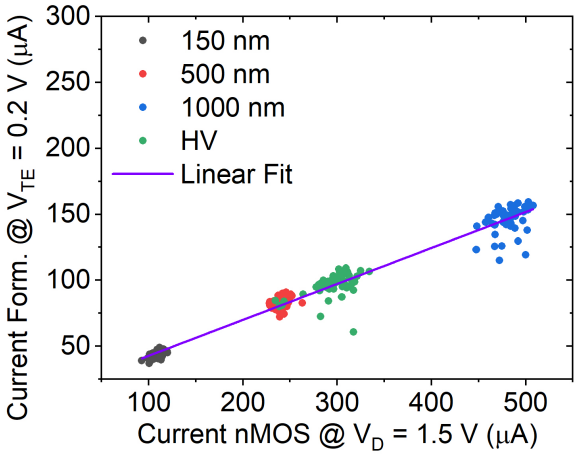


Figure 2. Read-out current at Vte = 0.2 V for the conductive level programmed into the 1T1R cell during Forming vs the current value provided by the corresponding nMOS at Vd = 1.5 V, for every transistor size.

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Programming of artificial synapses in neurotransistors without direct gate node access

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Among the various hardware implementations of artificial spiking neurons, the neurotransistor [1], [2] is a recent concept where the input stage of a leaky integrate-and-fire (LIF) artificial neuron is implemented by connecting a memristor to the gate of a metal-oxide-semiconductor field-effect-transistor (MOSFET). The memristor, its intrinsic parallel capacitance (assuming a metal-insulator-metal structure) and the gate-to-bulk capacitance of the MOSFET together form a pseudo-memcapacitive subcircuit which determines the charge integration rate of the LIF neuron. While the neurotransistor shows promise as an artificial neuron due to its compact size, simplicity and direct inclusion of synaptic functionality in the device, several challenges still remain.

How to program the different states of the memristor is one of these challenges, especially in the case with a single memristor in series with a MOSFET gate, since typically a large enough current needs to flow through the memristor during programming. One solution is connecting the drain of a secondary MOSFET to the floating gate, as is depicted in Fig. 1a. The second MOSFET would provide an alternate path for the current through the memristor when it is switched on. However, when considering an integrated device with the MOSFET in the front-end-of-the-line (FEOL) and the memristor in the back-end-of-the-line (BEOL), an additional transistor in the FEOL would severely limit the area-efficiency of the neurotransistor. This is especially problematic when considering e.g. spiking neural network applications with many neurotransistors in parallel.

In this work, we propose an alternative solution for artificial synapse programming in the neurotransistor where the gate can remain floating and the FEOL area can be constricted to just a single MOSFET. This is achieved through integrating multiple memristors in parallel in the BEOL (Fig. 1b), which enables memristor programming through resistive voltage division between the target memristor and the other parallel memristors. In simulation, we demonstrate the effectiveness of this method using a dynamic compact model of an analog switching Ti/Al2O3/NbOx/Ti resistive random-access-memory (RRAM) device fabricated at NaMLab gGmbH [3], with eight RRAM devices in parallel. Here, two cases are considered: the BEOL with all RRAM devices originally in a high resistance state (Fig. 2a, Fig. 2c and Fig. 2e), and with all RRAM devices originally in a low resistance state (Fig. 2b, Fig. 2d and Fig. 2f). As is apparent from Fig. 2e and Fig. 2f, in both cases, through careful selection of applied voltages, we achieve less than 0.02 % state change in the parallel RRAM devices after 25 set-reset cycles of the target RRAM device. We note that since half of the devices are connected with the bottom electrode to the gate, and half with the top electrode to the gate, any eventual asymmetry in memristance depending on the sign of the memristor voltage drop can be taken into account, and any of the RRAM devices can be programmed. This investigation further solidifies the neurotransistor as a competitive choice for a LIF neuron input stage implementation.

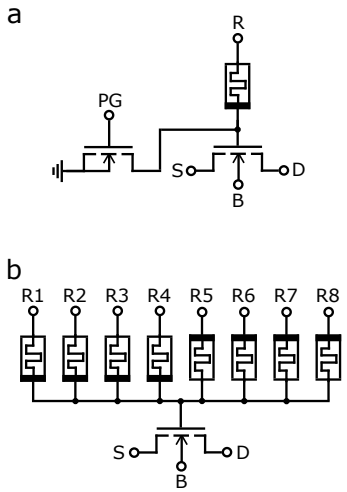


Figure 1. The neurotransistor circuit with two different methods of memristor programming. (a) a secondary MOSFET connected to the floating gate, where opening the MOSFET through applying a positive bias on PG would allow the memristor to be programmed through an appropriate voltage on R. (b) Our proposed programming scheme with eight memristors connected in parallel in the BEOL. R1-R4 and R5-R8 have opposite orientations.

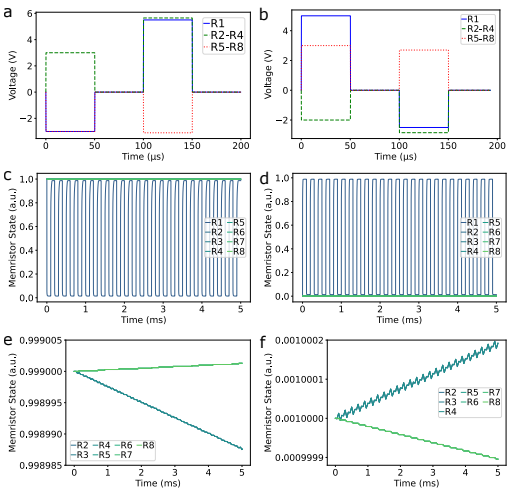


Figure 2. Simulation results of programming memristor R1 in Fig. 1b through voltage division with R2-R8. (a) The voltages applied to R1, R2-R4 and R5-R8 during the first two set and reset operations when all memristors are in a high resistance state, and (b) during the first two reset and set sequences when all memristors are in a low resistance state. (c) The memristor states when applying the pulse sequence in (a) 25 times, and (d) when applying the pulse sequence in (b) 25 times. (e) The memristor states as in (c) but without R1. (f) The memristor states as in (d) but without R1. We note in (e) and (f) that the state change across the programming cycles is less than 0.02 %.

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Talks

Oscillators

A Novel Spectral Method to Investigate Symmetry Breaking in Cellular Systems

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Symmetry breaking is an ubiquitous instability phenomenon, resulting in the formation of static and dynamic patterns, in excitable cellular media. It has attracted the interest of various luminaries, including Prigogine, Turing, Schrödinger, and Smale, over the past few decades. Despite their undoubted talent, however, these scientists were unable to understand the origin for these emergent effects ([1], [2]).

In a seminal work at the beginning of the new millenium [3], however, L. Chua demonstrated that a physical system may admit complex spatio-temporal solutions if and only if some of its constitutive elements are able to act as sources of infinitesimal energy about stable bias points, a condition for which they are said to operate on the Edge of Chaos.

In fact, as demonstrated in [4], homogeneous cellular media may only undergo diffusion-driven instabilities, resulting in pattern formation, if the basic cell is poised on the Edge of Chaos [3].

In this presentation we introduce a novel Frequency-Domain Method [5], based on powerful concepts from Control Theory, to investigate the bifurcation mechanisms, underlying the appearance of symmetry-breaking instabilities in cellular systems, as in the example from Fig. 1 [6]. The method is applicable to arrays of reaction cells, admitting distinct topologies, and coupled through different synaptic coupling arrangements.

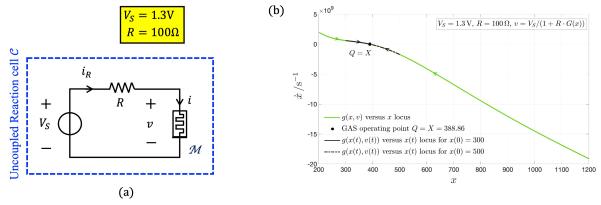


Figure 1. (a) Basic reaction cell. (b) Its State Dynamic Route (SDR) for V_S=1.3V and R=100Ω [asc22b].

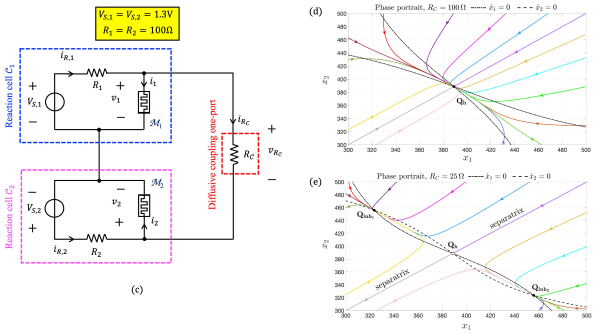


Figure 2. (c) Reaction-Diffusion Cellular Ceural Network. (d) ((e)) Its Phase Portrait in a scenario preceding (following) the symmetry-breaking phenomenon, where, particularly, R_C=100Ω (R_C=25Ω). The homogeneous static solution of the two-cell array is destabilized for R_C=49.7Ω, when a Pitchfork Supercritical Bifurcation gives origin to two locally-stable inhomogeneous static solutions [asc22b].

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Self-Sustained Oscillation Driven by Colossal Emergent Inductance in a Molecular Memristor

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Memristors have attracted considerable attention as fundamental circuit elements for neuromorphic computing and unconventional electronic devices. Among their emerging functionalities, self-sustained oscillation has recently been observed in several memristive systems, offering new opportunities for oscillator-based computing and artificial neuron applications. However, the physical mechanism underlying memristive oscillation remains largely unexplored.

Here, we investigate the quasi-one-dimensional molecular Mott insulator $[Ni(chxn)_2Br]Br_2$ (chxn = cyclohexanediamine), which exhibits memristive behavior characterized by a pinched hysteresis loop (PHL) and negative differential resistance (NDR). Through impedance spectroscopy, we recently identified a colossal emergent inductance reaching approximately 145 kH in this system (Fig. 1), several orders of magnitude larger than those of conventional inductive components [1]. This inductive response emerges in the same temperature and bias regions where pronounced memristive characteristics are observed, suggesting a close relationship between the internal electronic dynamics and the memristive state.

To test whether the colossal emergent inductance can drive oscillatory dynamics, we connected an external capacitor in parallel with the memristor. Above the NDR threshold current, stable self-sustained oscillations emerged without any physical inductor in the circuit (Fig. 2(a)). The oscillation frequency exhibited systematic dependence on capacitance, bias current, and temperature, enabling an independent estimation of the effective inductance from the oscillatory dynamics. Remarkably, the obtained inductance showed excellent agreement with that determined from impedance spectroscopy, providing direct evidence that the colossal emergent inductance is responsible for the oscillatory behavior.

These results provide direct experimental evidence that colossal emergent inductance drives self-sustained oscillation in a molecular memristor. The observed agreement between dynamic and spectroscopic estimates of inductance establishes a direct link between emergent circuit elements and nonlinear oscillatory dynamics in correlated-electron systems. More generally, these findings suggest that emergent inductance may be an intrinsic consequence of the state-variable dynamics responsible for PHL in memristive systems. In the presentation, we will further discuss how the addition of a simple series resistor transforms the oscillatory state into spike-like firing dynamics, highlighting the potential of molecular memristors for neuromorphic hardware (Fig. 2(b)).

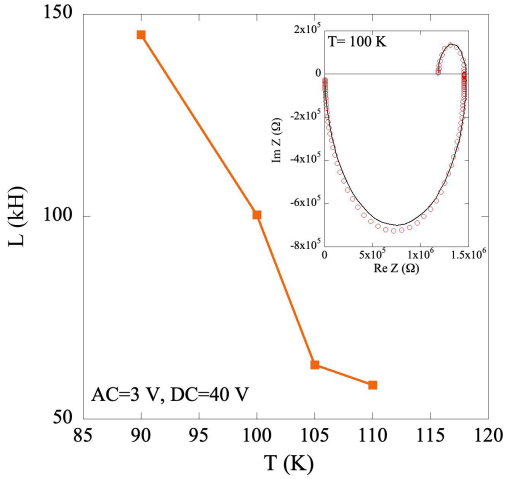


Figure 1. Temperature dependence of the emergent inductance in $[Ni(chxn)_2Br]Br_2$ (up to 145 kH). Inset: Cole–Cole plot at 100 K.

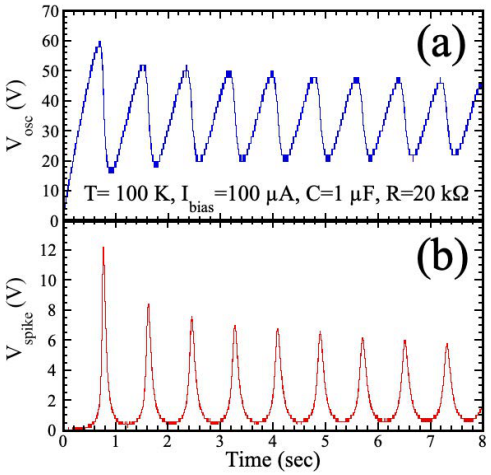


Figure 2. (a) Self-sustained oscillation and (b) spike-like firing in $[Ni(chxn)_2Br]Br_2$.

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Light-Modulated Oscillatory Neuromorphic Devices Using Phase-Transition V_3O_5

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Spiking neural network-based accelerators are crucial hardware components for artificial intelligence, enabling tasks such as computation, image analysis, and pattern recognition[1-2]. While volatile memristors based on transition-metal oxides can generate energy-efficient oscillation spikes making artificial spiking neurons, they typically require an initial electroforming step, negatively impacting device reliability. They also lack intrinsic optical sensitivity, necessitating external photodiodes to enable optical input. In this talk, we will present our recent development of a photo-sensitive oscillation neuron based on the phase-change-material V_3O_5, which undergoes an insulator-to-metal transition (IMT) when heated to 430 K [3]. We fabricated photo-sensitive two-terminal memristor devices using polycrystalline V_3O_5 films and investigated their distinctive electrical and optoelectronic properties through illumination-dependent electrical measurements, conductive-AFM, in-situ thermal imaging, and lumped-element modeling. Our devices exhibit electroforming-free volatile threshold switching and sensitivity to broad optical illumination, ranging from visible to near-infrared. Importantly, we show that the switching parameters and spiking frequency of the devices can be tuned by varying the light wavelength and intensity. Our analysis reveals that the changes in switching parameters result from both the photoconductive and bolometric properties of V_3O_5, which increase the overall conductivity of the oxide film and ultimately affect oscillation dynamics. This approach eliminates the need for external photodetectors, paving the way for compact, scalable, and energy-efficient oscillators that enable direct optical input into spiking neural networks, with potential applications in autonomous driving and robotic vision.

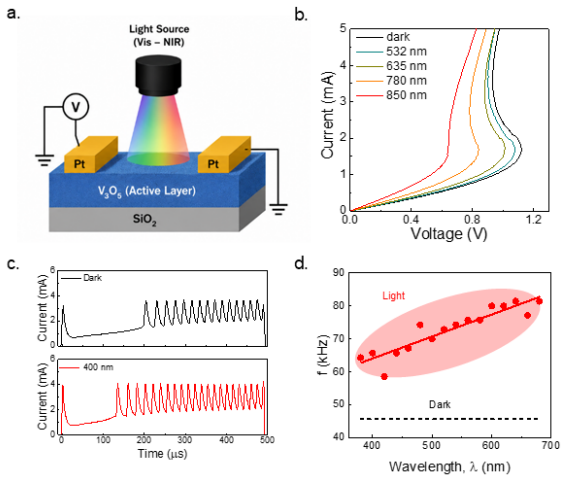


Figure 1. (a) schematic of the device structure (b) quasi-static current- voltage characteristics showing light-tunable negative differential resistance (c) light-tunable oscillation dynamics and (d) oscillation frequency as a function of incident light wavelength.

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Material Functionality

1P–1R Device for Optical Encoding and Edge-AI In-Sensor Computing

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Emerging edge-AI systems require integrated sensing, memory, and computing hardware to reduce data movement and energy consumption, particularly for vision applications that generate large volumes of image data [1]. Hybrid photodiode–memory architectures are attractive for in-sensor computing, combining optical sensing, programmable memory, and computation within a compact device footprint [2].

Here, we present a 1P–1R device integrating an MBE-grown GaAs photodiode with a sputter-deposited TaOx -based RRAM. The n-side of the photodiode is connected to the RRAM bottom electrode, enabling RRAM SET in reverse bias and RESET in forward bias (Inset, Fig. 1). The intensity-dependent photocurrent of the photodiode is used as the compliance current during RRAM SET process to achieve multilevel switching (Fig. 1). As a result, optical intensity is directly encoded into resistance states, enabling simultaneous sensing and storage of incident light information (Fig. 2). Beyond optical encoding, the programmable RRAM conductance serves as an analog weight for in-sensor processing. By selectively amplifying or attenuating photocurrents, operations such as contrast enhancement and motion detection are performed directly at the sensor level.

The proposed 1P–1R architecture provides a compact platform for integrating photodetection, memory, and computation, offering a promising route toward highly parallel and energy-efficient edge-AI In-sensor computing.

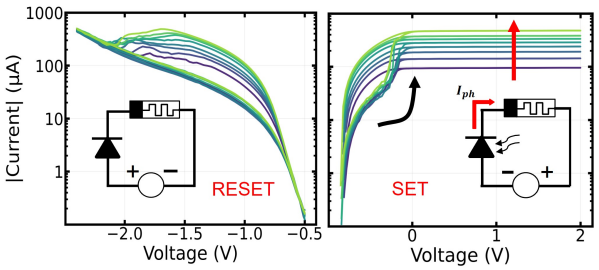


Figure 1. I–V characteristics of the 1P–1R device during SET and RESET operations. Insets show the circuit configurations used for programming. The photodiode reverse-bias current modulated by illumination-intensity acts as the compliance current during SET.

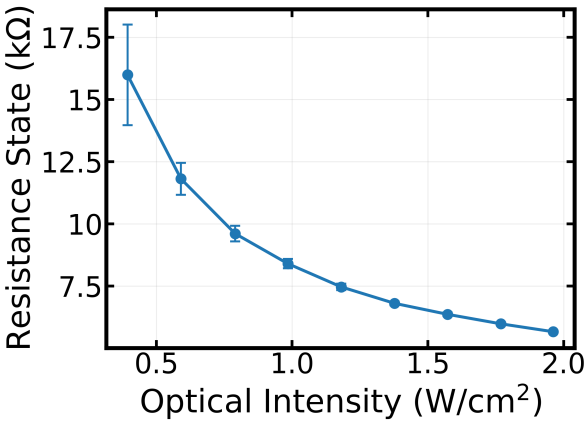


Figure 2. RRAM resistance as a function of illumination intensity, demonstrating direct optical encoding of light information into programmable multilevel resistance states.

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Analysis and Modelling of Undesirable Set in Resistive Random Access Memory (RRAM)

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Resistive random-access memory (RRAM) is a leading candidate for next generation scalable, embedded non-volatile memory, yet practical devices remain constrained by non-idealities such as device-to-device and cycle-to-cycle variability. Here we investigate an anomalous switching event, termed the undesirable SET, in which the conductive filament strengthens (sets) precisely when it is expected to dissolve (resets). We first experimentally observe this effect in an Au/Ti/SiOx/Mo RRAM stack, in which quasi-static reset sweeps reveal a reproducible, unexpected current jump followed by an elevated plateau, before the expected reset behaviour resumes. To resolve the underlying physics, we develop a 2-D axisymmetric multiphysics model in COMSOL that self-consistently couples electric current, heat transfer, and oxygen-vacancy transport, the latter combining field-driven drift, Fickian diffusion, and Soret diffusion, with the local electrical and thermal conductivities tied dynamically to the evolving vacancy field. [1]We show that flux terms alone cannot reproduce the filament strengthening, since drift dominates diffusion by more than an order of magnitude; a field- and temperature-activated Frenkel-pair generation source is therefore physically necessary.[2] Vacancy depletion at the SiOx/Ti interface concentrates the local field and Joule heating, thermally regenerating vacancies within the gap, refilling the filament, and producing the observed current jump. The resulting framework reproduces the bipolar switching characteristics of RRAM and captures the transient vacancy-regeneration event that underlies the undesirable SET.

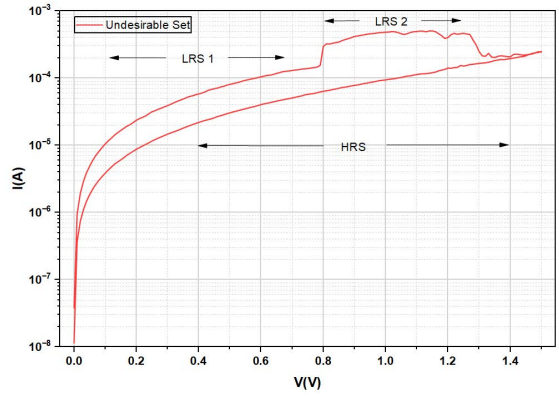


Figure 1. Representative I-V characteristics of an undesired SET during RESET, revealing three distinct resistance states: LRS1,LRS2 and HRS.

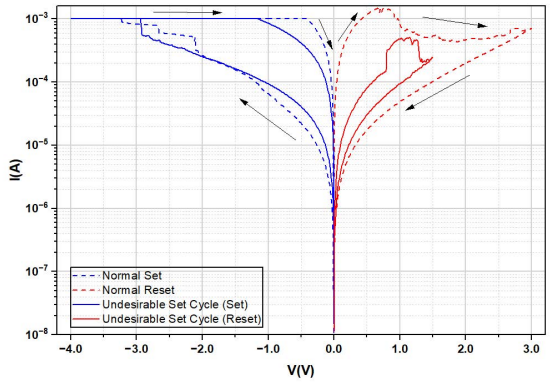


Figure 2. Normal switching cycle(dashed line) and Undesirable Set cycle(solid line)

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Capacitive-Memristive Coupling in Two-Dimensional Nanofluidic Systems for Adaptive Ionic Memory

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Nanofluidic memristors based on confined ionic transport offer a promising route toward bio-inspired computing, where memory and signal processing emerge from ion redistribution rather than purely electronic switching.[1-4] However, the interpretation of non-ideal hysteresis responses, including shifted, non-pinched, and multi-crossing current-voltage characteristics,[5] remains challenging because both ionic memory and capacitive effects can contribute to the measured response.

Here, we investigate the interplay between memristive ionic transport and capacitive coupling in two-dimensional Ångström-scale nanofluidic channels. By controlling the electrical driving conditions and the surrounding circuit environment, we observe a continuous evolution of ionic hysteresis from intrinsic memristive behaviour toward capacitively coupled response states. This transition indicates that the apparent memory signature of confined ionic systems is not governed solely by ion-channel interactions, but also by the relaxation timescale of ions and the capacitive context of the measurement circuit. A minimal dynamical framework is used to rationalize the observed trends by treating the measured current as a combined contribution from state-dependent ionic conduction and capacitive displacement current. This approach captures the qualitative transformation of hysteresis profiles and provides a unified picture of how frequency, ionic relaxation, and external circuit loading reshape nanofluidic memory behaviour. We further show that capacitive coupling can modulate the temporal response of the system, enabling adaptive memory retention and rate-dependent firing behaviour relevant to neuromorphic functions.

These results highlight capacitive-memristive coupling as a key design parameter in nanofluidic neuromorphic devices. More broadly, the work suggests that engineering both the confined ionic pathway and its circuit environment can provide deterministic control over memory, plasticity, and neuron-like dynamics in aqueous iontronic systems.

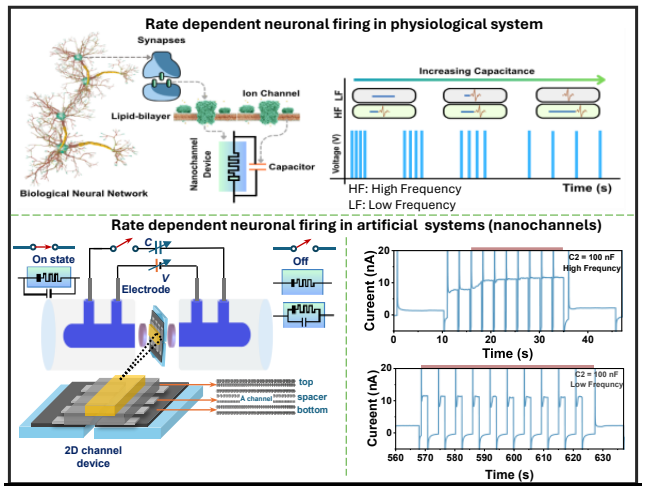


Figure 1. Bio-inspired rate-dependent firing in capacitively coupled Ångström-scale nanofluidic channels. The schematic compares synaptic ion-channel activity in biological neural networks with voltage-driven ionic transport through artificial nanofluidic channels. When a parallel capacitor is connected to the device in the on-state circuit configuration, the ionic relaxation dynamics are modified, leading to capacitance- dependent changes in spike timing and firing rate.

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CNT FET for heterosynaptic applications

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Synaptic devices can be used to build neural networks on hardware to perform various cognitive tasks when properly trained, like ANN programs at the software level. This will help to address the Von Neumann architecture bottleneck, where significant energy is wasted in moving data back and forth between the memory unit and the processing unit in AI data centres. We have fabricated a heterosynaptic CNT (Carbon nanotube) FET in which the channel material's conductance is dependent on the gate electric field. In our device, we apply presynaptic input pulses at the drain terminal, but the CNT FET can achieve different conductance states only when the gate electric field is applied. In the absence of a gate electric field, the CNT FET loses conduction modulation. For device fabrication, we patterned the Ni electrodes on the SiO_2/Si wafer using photolithography and lift-off. This step is followed by the spray-coating of CNT onto Ni electrodes. The backside of the SiO_2/Si wafer is etched with HF to create the gate contact. Characterization techniques, such as Raman and FESEM, are performed on the device's planar surface to assess the morphology and purity of the semiconducting CNT sprayed onto it. Several electrical characterizations have also been performed, which are categorized into two sections: (i) DC study and (ii) pulse study. In the DC study, we examined the device's output and transfer characteristics. In the output characteristics, we have applied multiple dual sweeps of voltage (0 V to -10 V to 0 V) up to 30 consecutive cycles. It is observed that, with each dual sweep, channel resistance decreases when the gate electric field is effective. This decrease in conductance is pronounced at high gate bias (∼40 V). In the pulse analysis, the gate bias is maintained at 10 V, and a train of 5 V, 100 µs pulses is applied as a presynaptic input at the drain terminal. With each presynaptic pulse, the device's conductance decreased, indicating depression, and it naturally recovered to its initial conductance state in milliseconds once presynaptic pulses are stoped. This behavior indicates the device's short-term plasticity, which can be used for applications like speech recognition, information filtering, and real-time processing.

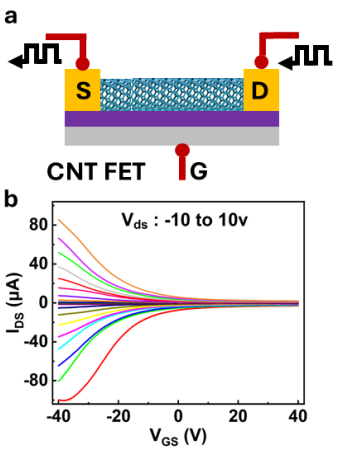


Figure 1. (a) Device schematics and (b) Transfer characteristics showing the p-type nature of CNT.

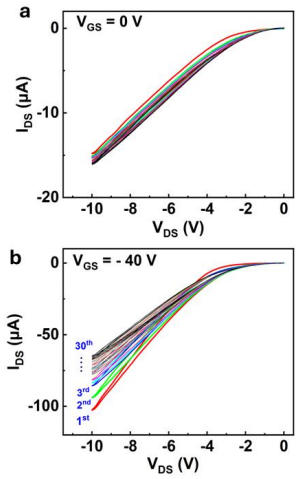


Figure 2. Dual V_{DS} sweeps upto 30 cycles when the applied gate bias is (a) 0 V and (b) 40 V.

Compact Modeling of Trap-Assisted Tunneling in Area-Dependent PCMO Memristive Devices

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Memristive devices based on transition metal oxides are considered promising candidates for next-generation non-volatile memory and emerging computing systems due to their scalability, analog switching behavior, and compatibility with neuromorphic applications [1]. Among various device concepts, area-dependent valence change memory (VCM) cells exhibit gradual resistance modulation and multi-level switching characteristics, making them particularly attractive for information storage and in-memory computing architectures [2]. In this work, we investigate the conduction and switching mechanisms of a bilayer VCM device incorporating hole-doped Pr1-xCaxMnO3 (PCMO). Physics-based compact models were developed to describe trap-assisted tunneling (TAT) transport through the insulating layer. Two transport scenarios, referred to as TAT-E and TAT-H (Fig. 1), were implemented in MATLAB and systematically evaluated by comparing simulated current–voltage characteristics (Fig. 2) with experimental measurements. The results reveal that the hole-based transport model accurately reproduces the observed bipolar switching polarity and area dependence, indicating that hole-tunneling dominates the conduction process in the investigated devices. In addition, transient simulations were performed to analyze SET dynamics, resistance evolution, and potentiation / depression behavior under pulse stimulation. To further improve computational efficiency and provide deeper physical insight into TAT transport, a new model based on Gaussian trap density-of-states distributions is currently being developed. By approximating the dominant transport contribution around energetically and spatially favorable trap states, the model significantly reduces computational complexity while preserving the essential transport physics.

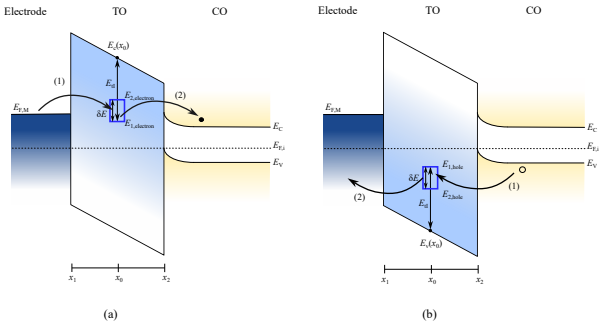


Figure 1. Schematic illustration of the two compact trap-assisted tunneling transport models: (a) TAT-E and (b) TAT-H.

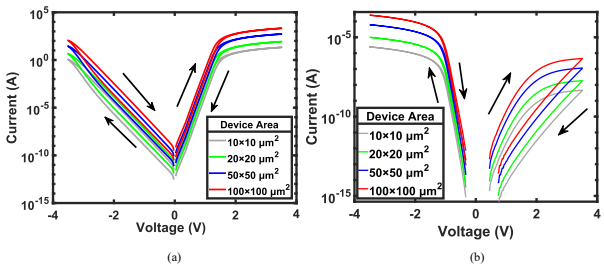


Figure 2. Simulated current–voltage characteristics of the (a) TAT-E and (b) TAT-H models for different device areas.

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Controllable and multi-timescale relaxation dynamics of Ag/SiOx/Pt volatile ECM memristors with an Al2O3 nanolayer at the active interface

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The rise of memory-heavy workloads, such as artificial intelligence, is driving the necessity to develop new computational paradigms to lower the power consumption of the information technology infrastructure. Conventional computers, based on the Von Neumann architecture, rely on two physically separated devices to store (memory units) and analyze (compute units) data, and this leads to inefficiencies related to data transfer in the bus. Neuromorphic computing proposes to develop computational systems that emulate the intrinsic efficiency of a brain-like structure. To implement neuronal and synaptic primitives in electronic systems, it is necessary to have electronic devices that show complex and controllable dynamical timescales to simulate short-term and long-term plasticity and neuronal functions. One of the most promising devices for this role is the volatile electrochemical metallization memristor. After the application of a voltage stimulus that causes the transition from a high resistance to a low resistance state, due to the formation of a conductive filament, this device spontaneously reset in a tunable time interval, called retention time. [1]

Our work investigates the complex relaxation dynamics of Ag/SiOx/Pt volatile ECM devices, in particular emerging from the insertion of a nanometric ALD-deposited Al2O3 layer between the Ag active electrode and the SiOx electrolyte. The reference Ag/SiOx/Pt stack already shows interesting integrative effects over short timescales [2], but the insertion of the alumina layer further enhances the dynamical timescales of the device. We analyzed, thanks to quasi-static electrical characterization, three different material stacks (Ag/SiOx/Pt, Ag/1 nm Al2O3/SiOx/Pt and Ag/2.5 nm Al2O3/SiOx/Pt) and we focused on the effect of programming conditions and alumina layer thickness on relaxation dynamics of the devices. As shown in Fig. 1, Al2O3 layer insertion increases retention time of at least one order of magnitude and, furthermore, causes cumulative effects, which are not present on the investigated timescale in bare Ag/SiOx/Pt samples. In fact, retention time increases with the number of set – spontaneous reset cycles in a cumulative way even if after each cycle the device returns to the high resistance state. The insertion of Al2O3 increases both the intrinsic retention (i.e. the retention time of a device in a pristine condition, without accumulation) and the cumulative retention (final retention after the same programming sequence) and the increase is higher for thicker Al2O3 interlayer. Cumulative effects are, however, reversible, as shown in Fig. 2: if a long enough hold time (thold) is left for the device to recover between cycles, cumulative effects can be eliminated, recovering intrinsic retention and the pristine state. This recovery time, together with cumulative effects, increases drastically with alumina layer thickness.

Through material engineering, we (i) increase time constants and (ii) enrich the bare SiOx devices with cumulative effects and recovery time. All these results give access to unexplored physics of the devices and can be exploited to implement time-dependent brain-inspired computation.

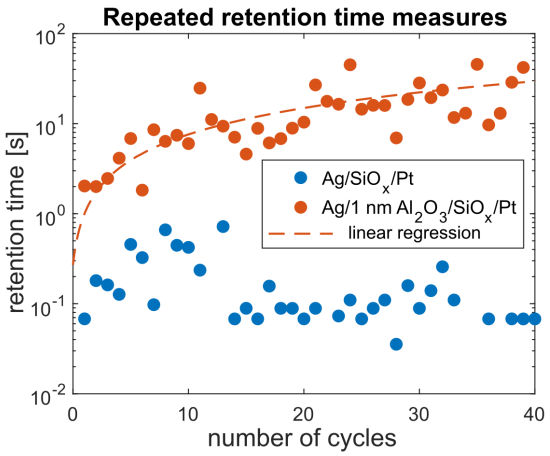


Figure 1. Effect of Al2O3 layer introduction on retention time. The device with 1 nm Al2O3 (in orange) shows longer intrinsic retention time and cumulative effects.

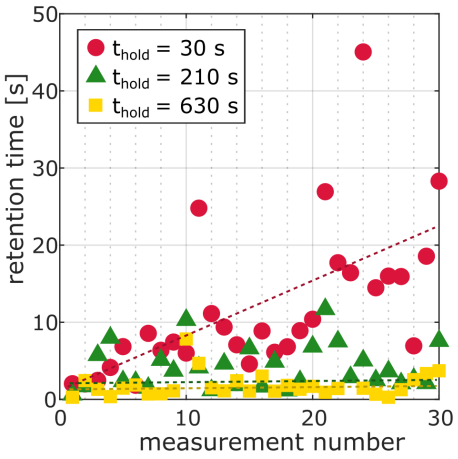


Figure 2. Effect of hold time on cumulative effects 1 nm Al2O3 device. For short hold time (in red) cumulative effects are present. For longer hold times (in green and yellow) they are eliminated.

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Electrochemical random-access memory devices for neuromorphic computing

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Oxygen-based electrochemical random-access memories (O-ECRAMs) are attracting great interest for in-memory and neuromorphic computing approaches in AI inference and training applications. O-ECRAM are three terminal resistive memory devices in which the application of a voltage to the gate terminal allows the analog modulation of the channel resistance, measured through the drain-source terminals. This resistance modulation is obtained by the injection of ions into the channel, acting as dopants that modify its electronic conductivity. Thanks to the three terminal (3T) structure and the non-filamentary switching mechanism, O-ECRAMs deliver low read/write power consumption, highly precise and gradual control of channel conductance, low device variability, compatibility with CMOS back-end-of-line processes, and the potential for three-dimensional (3D) integration [1]. Despite the recent advancements in literature, there are still open points related to materials and electrical properties co-optimization in terms of retention, switching speed and scaling. Furthermore, the exact nature of the switching mechanism (bulk or interfacial) and the role of oxygen and/or protonic effects in O-ECRAM is under discussion.

In this work, we engineer WOx/HfO2/WOx O-ECRAMs by investigating the effect of HfO2 electrolyte thickness and deposition techniques, post deposition thermal treatments and device geometry on the electrical performance (e.g. programming speed, retention).

Fig. 1 shows the cross-sectional sketch of the O-ECRAM stack we fabricated. We studied the DC and pulsed characteristics of devices fabricated with and without the upper WOx reservoir layer, and varying channel length/width (in the 5 to 20 µm range). Fig. 2a shows the potentiation and depression curves of IDS (VDS=100 mV), in response to trains of positive and negative rectangular voltage pulses applied to the gate respectively. Fig. 2b shows the mean ΔG variation as a function of the programming pulse, which is in agreement with previous studies on O-ECRAM [2].

We obtained a DC conductance variation of up to 4 orders of magnitude, depending on the sweep rate and voltage. Furthermore, we demonstrated that it is possible to achieve an overall linear and symmetric conductance variation from 0.2X to 10X, depending on the programming pulse duration and voltage amplitude, but with decreased linearity for wider windows. Moreover, we demonstrated the functionality of O-ECRAM at low voltage (down to 500 mV pulses), and with short pulses (in the µs range) at higher voltage amplitudes, although with a limited conductance variation. Furthermore, we assessed the device retention after programming and we identified two different behaviours: a short-term memory effect related to the return of the channel conductance to an equilibrium point, and another long-term effect related to the modification of this equilibrium point. Finally, our study provides valuable insights into the ionic transport in the electrolyte layer (drift) and the diffusion in the channel layer.

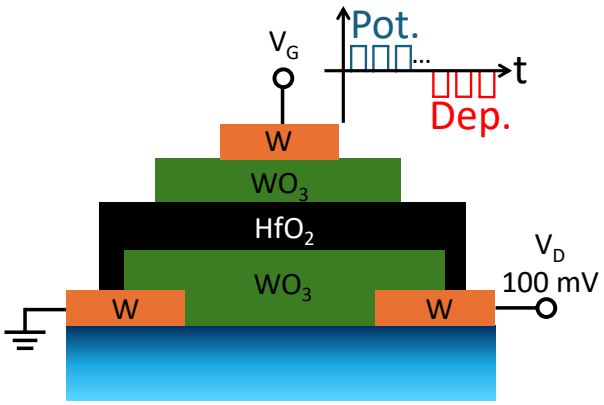


Figure 1. ECRAM material stack sketch. WO3 channel and reservoir, HfO2 electrolyte and W contacts.

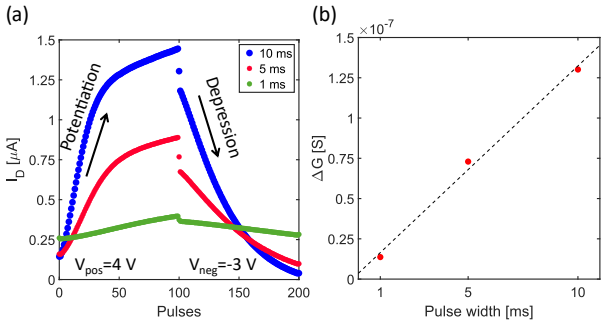


Figure 2. (a) Potentiation and depression curves obtained by the application of rectangular voltage pulses to the gate. (b) Mean conductance variation for each pulse as a function of the pulse width.

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Experimental Investigation and Modeling with COMSOL Multiphysics Software of Ag/ZnO/ITO Memristor

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In the current digital era, significant advancements have been made in memory systems and their speed and energy efficiency. Resistive-switching memristors based on oxide thin films are attractive candidates for nonvolatile memory which can be used in different applications like neuromorphic computing and spiking neural networks because of their simple device structure, low-power operation, and ability to retain distinct resistance states [1]-[3]. In this work, Ag/ZnO/ITO memristor devices were experimentally fabricated and analyzed together with a COMSOL Multiphysics model to investigate oxygen-vacancy-controlled resistive switching in ZnO.

The ZnO thin film was prepared on an indium tin oxide (ITO) coated glass substrate by spin-coating of a sol-gel from zinc acetate dihydrate, ethanolamine, and 2-methoxyethanol, followed by drying and annealing at 180°C [4]. Multiple coating cycles with 3000 rpm for 30 s each were used to form the desired ZnO active layer and Ag as a top electrode was deposited by sputtering process to complete the fabrication. Stylus Profilometer measurements confirmed the ZnO and Ag thicknesses of approximately 148 nm and 60 nm, respectively. Then, electrical characterization using a Keithley 2400 source meter and Python programming script was performed with Ag as a positive terminal and ITO as a negative terminal. The memristor devices showed a bipolar hysteretic I–V behavior as seen in Fig. 1. No electroforming was needed and the device exhibited a high ratio of electric resistances for the high and low resistance states: 6.9×10^{3} at +1.0 V and 1.5×10^{3} at +2.0 V, indicating pronounced resistive switching.

A 2D axisymmetric COMSOL Multiphysics model of the Ag/ZnO/ITO stack was developed to simulate the memristor with 60 nm thick Ag electrode, 150 nm thick active ZnO layer, and 30 nm thick ITO electrode. The Electric-Current (EC) and the Transport-of-Charge-Carriers (TCC) physics models in COMSOL were used to describe oxygen-vacancy migration in the memristor device. The model used normalized oxygen-vacancy concentration as a variable and linked ZnO conductivity to the oxygen vacancy concentration through a nonlinear conductivity expression. The conductivity of ZnO was expressed as an oxygen-vacancy-concentration-dependent function bounded between the high-resistance-state (HRS) conductivity of 7.26×10^{-7} S/m [5] and the low-resistance-state (LRS) conductivity of 10^{2} S/m limit, keeping the Ag and ITO electrode conductivity fixed (6.3×10^{7} S/m and $\sim10^{6}$ S/m, respectively). The TCC model used voltage-dependent rate of carrier density change to represent the transport of oxygen vacancy due to defect generation and trap filling. This strengthens the conductive path in the active layer under a positive voltage and weakens the conductive path under a negative bias. The simulated I–V response produced a pinched hysteresis with current in the mA range, which is consistent with the experimentally obtained results. From the I-V curve simulated in COMSOL Multiphysics (see Fig. 2), the ratio of electric resistances for the high and low resistance states was 46 at +1.0 V and 7.0 at +2.0 V.

The combined experimental and simulation results indicate that oxygen-vacancy-mediated conductivity modulation can describe bipolar switching in Ag/ZnO/ITO memristor devices.

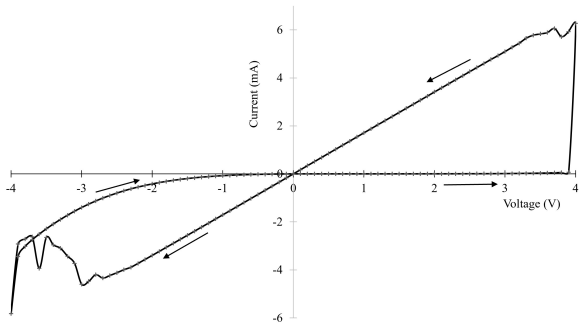


Figure 1. Experimental I-V pinched hysteretic characteristic of the Ag/ZnO/ITO memristor with the 148 nm ZnO thin-film layer.

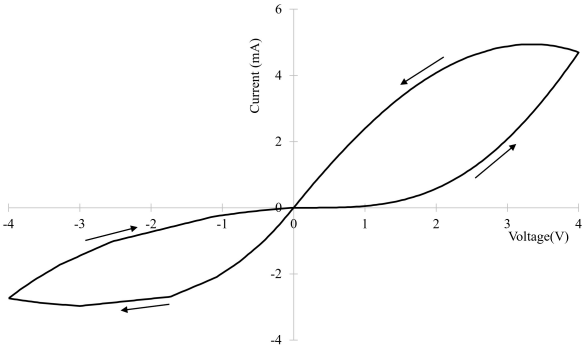


Figure 2. Simulation of I-V pinched hysteretic characteristic of Ag/ZnO/ITO memristor with the 150nm-thick ZnO layer using COMSOL Multiphysics software.

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Impact of Defect Density on Reset Voltage in Memristive Filaments: A Two-Dimensional kinetic Monte Carlo Study

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Memristors are widely regarded as a promising emerging technology due to their outstanding range of potential applications, such as memory, neuromorphic computing, cryptography, etc. [1]. However, the physicochemical mechanisms governing the resistive switching process remain only partially understood. The development of advanced simulation tools is therefore essential to elucidate these mechanisms.

In this work, we present a new simulation tool based on a two-dimensional kinetic Monte Carlo model, developed in-house, which enables the simulation of multi-filamentary resistive switching over the entire operation cycle, i.e., forming, reset, and set. Fig. 1 shows the simulation of a characteristic set (under positive bias) and reset (under negative bias) cycle for a TiN/Ti/Al2O3/W device of reference [2]. The simulation is initiated after the first forming and reset cycle. For this reason, a non-zero concentration of residual defects from the initial filaments remains within the insulator, as depicted in Fig. 1a. Since the probability of generating new defects is higher in the vicinity of existing ones, filament reconstruction occurs upon the application of a positive bias (see Fig. 1b–d). Under reverse bias, the generated ions drift back into the insulator and recombine with vacancies, resulting in filament rupture (see Fig. 1e). As expected, the thickest filament ruptures first because its lower resistance leads to a higher current flow and, consequently, to enhanced Joule heating.

Once the tool was correctly calibrated, we studied the effect of the defect density in the filament on the reset voltage. We simulated the reset process of a mono-filamentary structure, considering different filament maximum diameters and different defect concentrations in the filament. After a negative voltage ramp is applied, the reset voltage (Vreset) was calculated as the voltage at which the filament (the percolation path) breaks down. Fig. 2 shows the Vreset vs the defect density. The results suggest that the Vreset decreases as the defect density increases until 10 def./nm2, where the trend changes. At low densities, the filament is partially formed, so its resistance is high, and a higher voltage is needed to completely break it. As the density of defects increases, the filament gradually forms, but with weak points, i.e., localized narrowings. The linked resistance reduction and the presence of the weak points decrease the Vreset rapidly. For densities higher than 10 def./nm2, the number of weak points is close to zero because the filament is almost formed, so the Vreset is stabilized and only depends on the total resistance of the filament.

In summary, the proposed two-dimensional Monte Carlo tool provides a physically grounded framework to investigate multi-filamentary resistive switching in memristive devices, from defect generation and filament reconstruction to their eventual rupture under electrical stress. By quantitatively linking the reset voltage to the defect density and filament morphology, this approach offers valuable guidance for the design and optimization of memristor-based technologies.

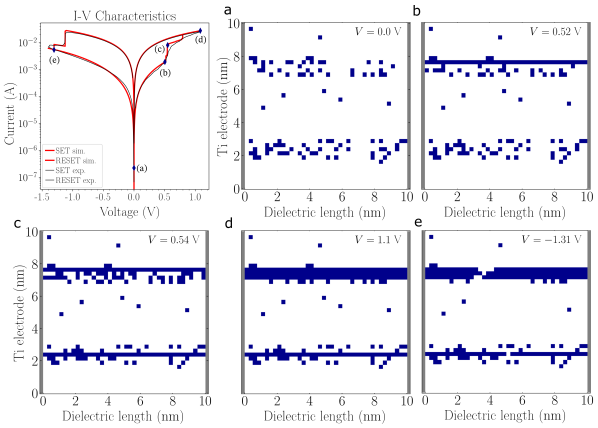


Figure 1. Monte-Carlo simulation of a set and reset cycle. The blue boxes represent the oxygen vacancies generated during the resistive switching process.

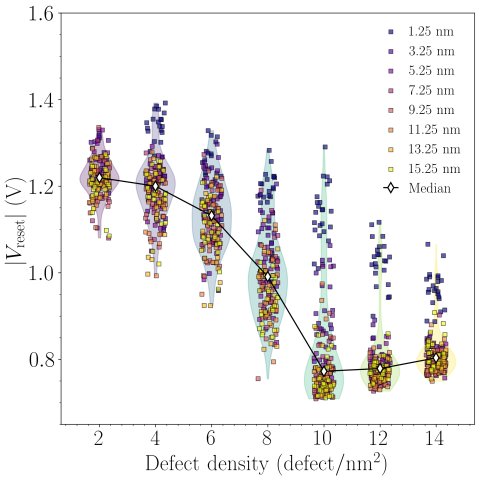


Figure 2. Reset voltage versus defect density in the filament for several maximum filament diameters.

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Influence of Experimentally Determined Thermal Boundary Conductance on Heat Dissipation in VCM Memristors: An Electro-Thermal FEM Study

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The resistive switching behavior of valence change mechanism (VCM) memristors is closely linked to localized Joule heating within nanoscale conductive filaments [1]. Accurate prediction of filament temperatures therefore requires a realistic description of heat transport across the multiple interfaces present in thin-film device stacks. However, thermal boundary conductance (TBC) values are commonly estimated from literature or treated as fitting parameters, introducing significant uncertainty into electro-thermal simulations.

In this work, we investigate the impact of interfacial heat transport on the thermal behavior of TiN/HfOx$_x$/Al filamentary VCM memristors using three-dimensional finite element method (FEM) simulations. Thermal boundary conductance values of the relevant interfaces were experimentally determined by frequency-domain thermoreflectance (FDTR) measurements and subsequently incorporated into the electro-thermal model. This approach enables a realistic representation of interface-limited heat dissipation within the memristive stack [1].

The simulations reveal a strong influence of the experimentally determined TBC values on the local temperature distribution and thermal confinement within the conductive filament. Variations in interfacial thermal transport significantly affect peak filament temperatures and heat spreading in the active device region, demonstrating that interface thermal resistance constitutes a key factor governing the electro-thermal operating conditions of VCM devices. The results further highlight the limitations of using idealized or literature-based interface parameters when assessing filament temperatures and switching-related thermal effects.

This study emphasizes the importance of experimentally characterizing interfacial thermal properties and incorporating them into electro-thermal models of memristive devices. The presented methodology provides improved predictive capabilities for thermal analysis and contributes to the optimization of future VCM-based memory and neuromorphic computing technologies.

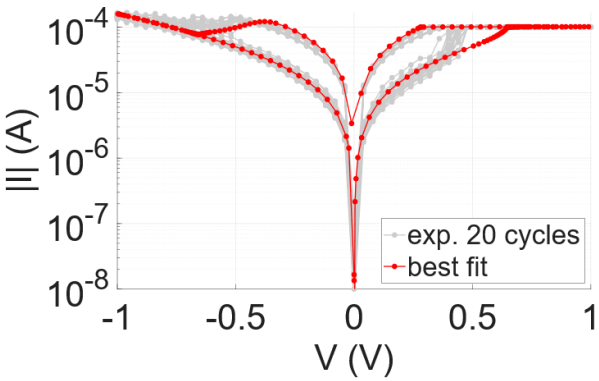


Figure 1. I-V: experiment and simulation for the 10s sweep

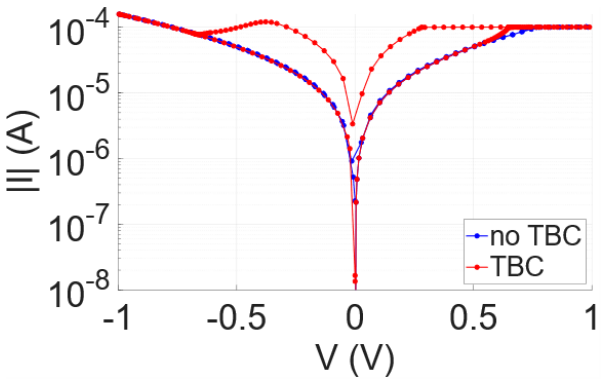


Figure 2. I-V: impact of TBC for the FEM simulation

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Integration of HZO Ferroelectric Weights on Flexible Substrates for Wearable Neuromorphic Systems

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In the context of wearable healthcare, embedding neuromorphic hardware onto flexible substrates has the potential to enable ultra-low-power, real-time biosignal processing directly at the sensor interface. Resistive, non-volatile memories based on ferroelectric HfO2/ZrO2 nanolaminates (HZO) implement synaptic weights in analog AI hardware modules [1]. We report on the transfer of HZO thin films from rigid wafers onto polymer supports. Using anodic release, we successfully detached the multilayer structure and re-deposited it onto a polyethylene terephthalate (PET) substrate. In this talk, we address the corresponding challenges, such as thermal stress management: the mechanical constraints induced by the resist bake might lead to curling of the membrane. Another challenge is the need for a sacrificial Al/Cr layer between the Si wafer and the functional stack: we discuss how it affects the crystallization of HZO. We successfully demonstrate non-volatile, analog resistive switching in TiN / HZO (5 nm) / WOx / TiN devices crystallized on W/Al/Cr/SiO2//Si wafers prior to the transfer. This work represents a step toward mechanically compliant ferroelectric weights suitable for integration in wearable neuromorphic systems. [1]

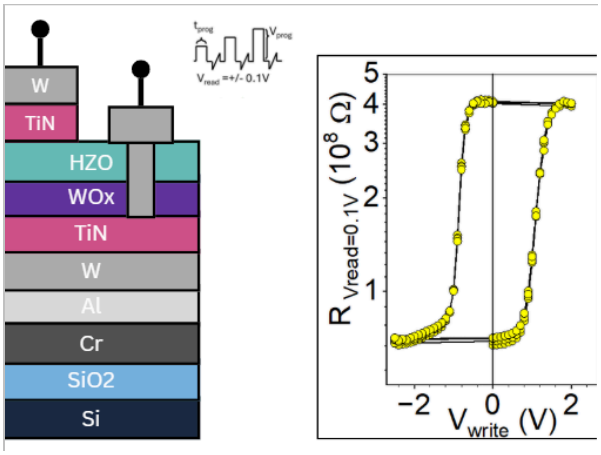


Figure 1. Left: Schematic cross-section of the TiN/HZO (5 nm)/WOx/TiN resistive memory device fabricated on a W/Al/Cr/SiO_2/Si stack prior to transfer. Right: Analog resistive switching characteristics measured at Vread=0.1 V, showing gradual conductance modulation as a function of the applied programming voltage

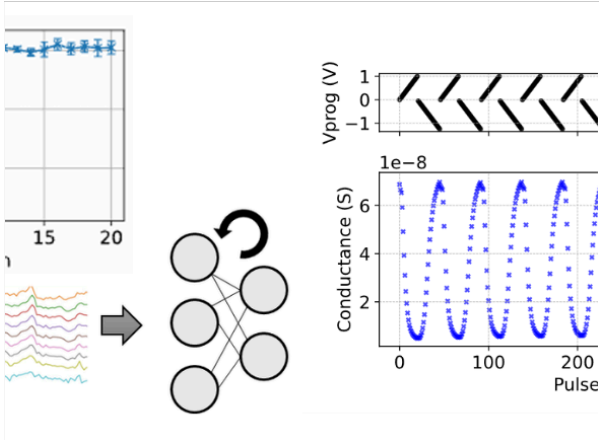


Figure 2. Left: System-level evaluation of the HZO-based analog memory devices for EEG classification using a neuromorphic inference framework. The measured long- term potentiation/depression (LTP/LTD) characteristics were used as synaptic weight update rules, resulting in a classification accuracy of approximately 80%. Right: Experimental LTP/LTD characteristics of the TiN/HZO/WOx/TiN devices under alternating programming pulses, showing gradual and repeatable

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Leaky-integrate functionality in GCMO-based neuromorphic devices

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Gd0.2Ca0.8MnO3 (GCMO)-based memristor devices were fabricated and their resistive switching properties were investigated. The standard resistive switching was demonstrated in devices with oriented single crystal GCMO phase as an active switching layer. The devices with polycrystalline phase showed pronounced volatility of the low resistance state towards a stable high resistance state. Combined with a non-binary analog SET control, volatile resistive switching provides a leaky-integrate function. Both the integration of SET and volatility of the respective low resistance were demonstrated and the results show potential for adopting partial neuron functions by using GCMO-based memristors.

The respective results were obtained for GCMO-based memristors deposited on MgO substrates and on SrTiO3 substrates, which generally are used for depositing epitaxial GCMO phase, by utilizing MgO buffer layer.

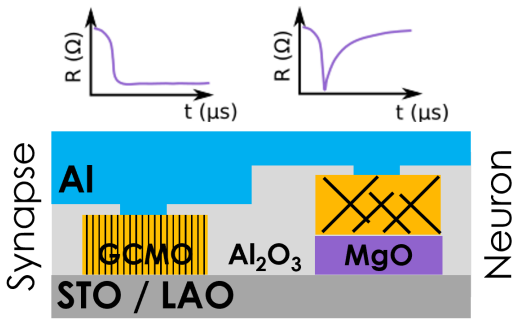


Figure 1. The structures of GCMO-based synapses and neurons.

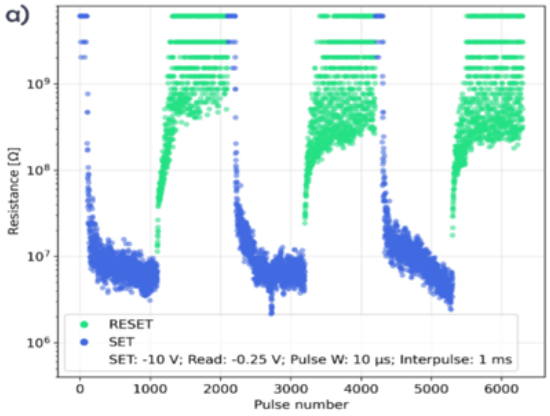


Figure 2. Neuronal leaky-integrate function measured on GCMO-memristor grown on MgO.

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Low-Frequency Noise Spectroscopy and Simulations as a Tool to Evaluate Oxide-Based Memristive Switching Mechanisms

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Low-frequency noise spectroscopy [1, 2] is a useful tool for studying resistive switching in oxide-based memory devices. In this work, we investigate HfO2 [3] and Y2O3-based RRAM and show how changes in the conductive filament affect both the device resistance and the current fluctuations. The results underline the value of noise measurements for identifying switching mechanisms and for judging the suitability of such devices for multi-level and analogue operation.

A clear noise–resistance relation is found and linked to the filament shape. In both samples, intermediate resistance states are mainly formed by an increase of the reoxidised filament gap. This leads first to a rise in noise with resistance, and then to a drop at high resistances. The latter behaviour is consistent with oxygen vacancies moving away from the most noise-sensitive region. Over a resistance range of six orders of magnitude, we observe a power law scaling that connects filament structure, defect arrangement, and noise magnitude SI(1Hz).

To support this picture, we combine experiments with a three-dimensional nonlinear resistor-network model. The model includes filament evolution, hopping-assisted transport, and spatially weighted fluctuators. It reproduces the coupled evolution of resistance and SI(1Hz), and shows how local filament changes and defect rearrangement shape the measured noise response. During DC cycling, HfO2 devices show a gradual reduction in noise in both high- and low-resistance states, consistent with filament stabilisation by oxygen-vacancy incorporation. Earlier works [4] on Y2O3, as well as new data, show a clear connection between noise and their resistance values.

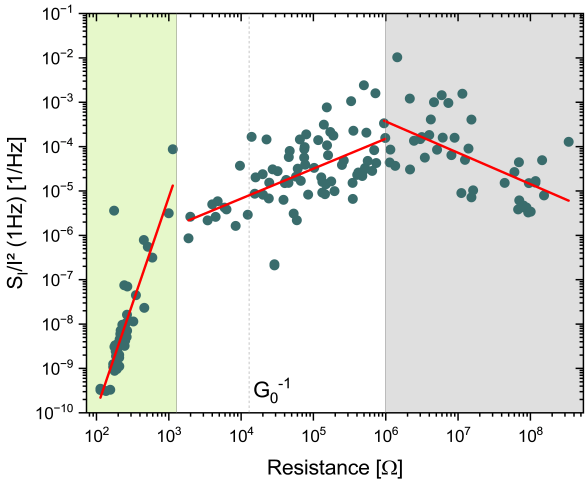


Figure 1. Three-stage power-law scaling of the normalized current noise magnitude at f = 1 Hz with the devices' resistance over a wide resistance range, including LRS, IRS and HRS

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MemrisTec Memristor Model Platform: An Open Educational Framework for Studying Memristive Devices

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Memristive devices have firmly established themselves as one of the most promising building blocks for next-generation electronics. Their ability to combine computation and non-volatile storage in a single nanoscale element makes them attractive for in-memory computing, logic-in-memory architectures, and neuromorphic systems inspired by the dense and energy-efficient processing of biological neural networks. Driven by this potential, the past two decades have produced a rapidly growing number of compact memristor models, derived from a wide variety of physical mechanisms such as filamentary, interface-type, phase-change, ferroelectric, and spintronic switching. Each of these models comes with its own equations, parameters, and preferred simulation language (most often SPICE or Verilog-A). For students entering the field, and for lecturers who would like to introduce memristor models in their classrooms, this heterogeneity has become a serious obstacle: relevant information is scattered across many publications and repositories, and bringing it together in a coherent, hands-on form requires considerable expert effort.

Here, we want to present the MemrisTec Memristor Model Platform [1], an open educational framework developed at the Institute of Circuits and Systems at TUD Dresden University of Technology within the German Research Foundation Priority Programme DFG SPP 2262 MemrisTec. The platform gathers recent compact memristor models, both those contributed by the MemrisTec consortium and further relevant models from the literature, into a single, consistent Python implementation, and invites students and interested newcomers to directly interact and play with them through a web-based interface. Rather than providing yet another written review, the platform offers hands-on experience: visitors stimulate selected devices with sinusoidal, triangular, or rectangular waveforms, adjust amplitude and frequency through sliders, choose how many periods are displayed, view several models on top of each other in different colours, and freely select the quantities shown on the x- and y-axes (for example, voltage, current, or internal state variable).

The platform is built on three pillars that together support a step-by-step learning journey. The Memristor Model Table gives a first overview of a representative selection of published compact models, including a short introductory video and a quasi-static I–V plot (overlaid on experimental data for each entry, if also published). The Model Simulator lets students and lecturers build personal intuition for the underlying physics by interactively exploring the parameter space, with the freedoms deliberately mirroring those of a real laboratory measurement. The Model Repository, hosted on a publicly reachable GitLab [2], contains every model as readable, object-oriented Python code that can be downloaded and run in any Python environment, supporting users who want to extend or embed the models in their own work.conductance

A future Circuits Simulator will add circuit-level use cases such as logic-in-memory operations, cellular neural networks, and crossbar matrix-vector multiplications, utilizeable in frameworks, e.g. snnTorch [3], AIHWKIT [4], NeuroSim [5], and NeuroPack [6]. Because the platform is fully open source, its long-term educational value can be sustained by any group with an interest in memristive electronics, even beyond the lifetime of its initial funding in MemrisTec.

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Memristive-capacitive coupling for higher-order plasticity and reservior computing

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Ionic materials can store electrical history through ion redistribution, interfacial polarization and charge transport, yet these processes are often treated as separate resistive and capacitive contributions. Here we show that an ultrathin covalent organic framework membrane with ordered nanopores couples these degrees of freedom within a single confined ionic material. Nanoconfined ion transport provides a memory-bearing conductance state, whereas interfacial charge accumulation provides a dynamic charge-storage state. Frequency-dependent current–voltage measurements, electrochemical impedance spectroscopy and a compact coupled-state model indicate that the device response cannot be described by conductance modulation alone. Instead, transport–storage coupling organizes a hierarchy of temporal regimes, including volatile response accumulation, persistent conductance modification, timing-dependent state modulation, sliding-threshold behaviour and downstream temporal computation. These results identify memristive–capacitive coupling as a materials design principle for adaptive ionic dynamics in nanoporous framework membranes.

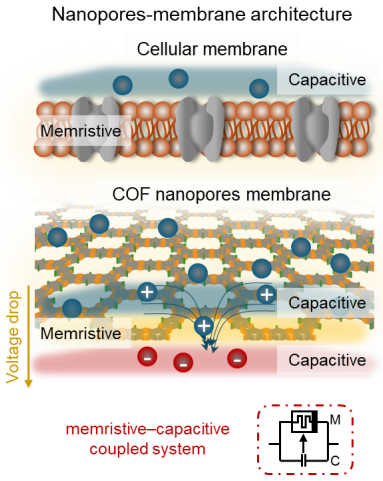


Figure 1. Nanopores-membrane architecture showing memristive-capacitive coupling

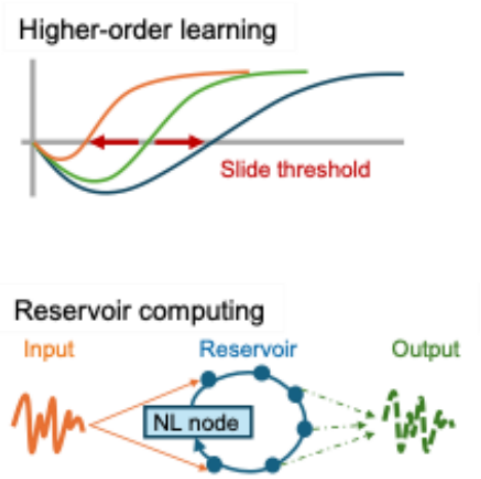


Figure 2. Higher-order learning and reservoir computing functions

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Multi-terminal Synapses and Neurons based on Floating-Gate Memory for Spiking Neural Network Implementation

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Traditional Von Neumann computing architectures face critical limitations in energy efficiency and data processing speeds, particularly for complex artificial intelligence tasks, due to the physical separation of memory and processor.

Spiking Neural Networks (SNNs) have emerged as a promising neuromorphic alternative, mimicking the brain's biological event-driven mechanisms to achieve ultra-low power consumption.

However, most existing hardware implementations of SNNs are based on conventional devices with a "single-input, single-output" structure. This structural limitation makes it difficult to realize the complex "many-to-many" connectivity between numerous neurons and synapses, which is essential for high-density neural integration.

In this study, we propose and implement multi-terminal synapses and neurons based on floating-gate memory technology. The multi-terminal structure was formed by fabricating multiple electrodes on a shared floating gate. Furthermore, the thickness of the Al2O3 tunneling insulator was precisely controlled via an Atomic Layer Deposition (ALD) process to differentiate the characteristics of neurons and synapses. We have successfully realized a hardware structure capable of simultaneous multi-terminal interactions.

The proposed multi-terminal design enables efficient signal transmission between multiple neurons and synapses within a compact area, significantly overcoming the connectivity constraints of traditional devices. This work provides a scalable and efficient hardware platform for the implementation of high-density, complex SNN architectures in next-generation neuromorphic systems

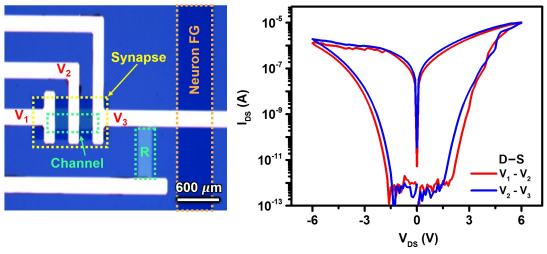


Figure 1. Device structure and electrical characterization. (a) Optical micrograph of the proposed multi-terminal device integrating a synapse and neuron. (b) IDS-VDS transfer characteristics measured between different terminal pairs.

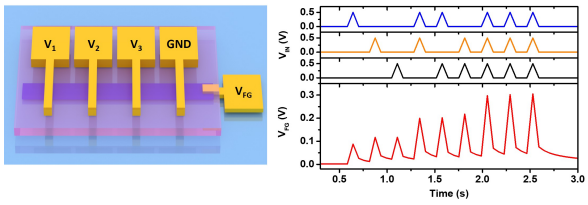


Figure 2. 3D architecture and spatial summation characteristics of the multi-terminal neuron. (a) 3D schematic view of the proposed neuron device. (b) Experimental demonstration of spatial summation.

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Multiphysics simulation of h-BN memristors, thermal and transient effects

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Memristors are being studied by the Industry and Academy because of promising applications connected to non-volatile memory ICs, neuromorphic engineering, hardware cryptography, and radio-frequency switches [1].

Here, we present results linked to devices based on the Au/Ti/h-BN/Au stack (see Fig. 1a). An h-BN multilayer grown by chemical vapor deposition (approximately 18 layers; see Figs. 1a and b) was placed on top of the bottom electrode via wet transfer. The I-V curves, obtained under ramped voltage stress, are shown in Fig. 1c. In Fig. 1d, the HRS and LRS resistances are shown versus cycle number. The inset shows the cumulative distribution function (CDF) of the same data, highlighting the cycle-to-cycle uniformity and a wide memory window. Several negative and positive voltage pulse trains have been applied to our devices to characterize pulse operation, after set/reset cycles to establish the initial device state. Both the pulse voltage and frequency have been changed to analyze the conductance modulation in depth.

A simulator of the devices under study has been built by means of COMSOL Multiphysics and MATLAB. The simulation domain is shown in Figs. 2a and 2b. The ultra-fine local mesh triangulation is critical for accurately solving the physical singularities at the Conductive NanoFilament (CNF) tip, such as intense electric field enhancement and extreme localized Joule heating gradients. A revolving device structure is employed to allow 3D simulations. The material physical properties are included: most data belong to the COMSOL material database, although some physical properties are changed following previous results in the literature. The Poisson and heat equations are solved in addition to the continuity equations in a 3D self-consistent approach. In this study, we consider an anisotropic thermal conductivity for the h-BN (a tensor in this case), and also an isotropic thermal conductivity for the sake of comparison. The experimental data are correctly reproduced as shown in Fig. 1c with the anisotropic thermal approach. Fig. 2c depicts how the Joule heat is generated by a single active cell, and the way the heat flux propagates in the dielectric and metallic electrodes. In the context of filamentary conduction, an accurate thermal description is essential.

A detailed analysis of the heat flux components and their dependence on the applied voltage during reset is shown in Fig. 2d. These distributions correspond to the simulated reset curve shown in orange symbols in Fig. 1c. We also simulated pulse operation both for set and reset events (Fig. 2e). This operation procedure allows for mimicking synapses with these devices by implementing depression and potentiation. Thermal effects can be engineered in these devices to facilitate the design of circuits, including these devices in the context of neuromorphic computing.

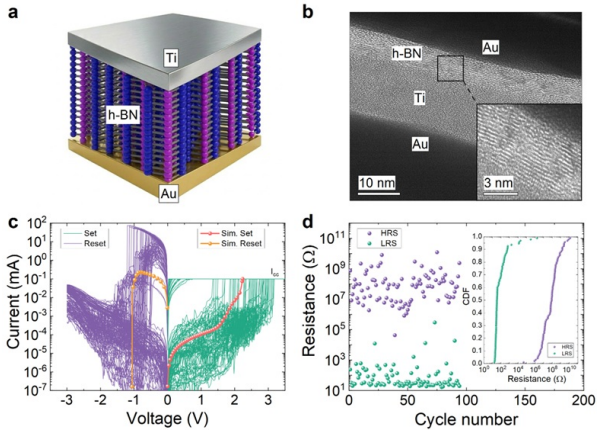


Figure 1. Device architecture and bipolar resistive switching characteristics of h-BN memristors. a Schematic illustration of the device stack structure, comprising a h-BN switching layer sandwiched between a Ti top electrode and an Au bottom electrode. b Cross-sectional high-resolution transmission electron microscopy (HRTEM) image of the fabricated Au/Ti/h-BN/Au stack. c Current-voltage (I-V) curves. The experimental set (green lines) and reset (purple lines) transitions are shown accompanied by their respective COMSOL simulated curves (red and orange symbols). d Endurance performance, evolution of the HRS (purple symbols) and LRS (green symbols) resistance (extracted at 0.15 V) across 100 consecutive switching cycles.

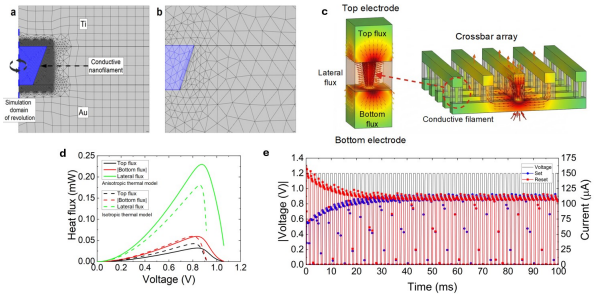


Figure 2. Simulation structure and mesh strategies. a Global view of the simulation domain in COMSOL assuming a revolving truncated-cone shaped CNF (blue region) with a highly refined mesh zone (dense dark region) within and surrounding the active switching volume. b Magnified view of the CNF interface and the corresponding mesh. c 3D visualization of localized Joule heating and heat dissipation pathways in a single device and in a crossbar array architecture. d Heat flux analysis in the h-BN memristor along a reset event. e Current and voltage versus time for pulse operation.

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Nanoscale Back-End-of-Line Silicon Carbide Memristor for Neuromorphic Computing

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Conductive-bridge memristors are promising candidates for neuromorphic computing, but their practical implementation requires dielectric materials that combine reliable resistive switching, synaptic tunability, and CMOS compatibility. Amorphous silicon carbide (SiC), a back-end-of-line (BEOL) material widely used in the CMOS industry, provides an attractive platform for scalable CBRAM-based neuromorphic devices.

In our previous work, we demonstrated that bilayer SiC/Si memristors can achieve one billion switching cycles with an ON/OFF ratio of ca. two orders of magnitude, and exhibit multiple resistive states switching by controlling the pulse conditions, proving the potential for high-performance applications [1]. We also demonstrated single-layer silicon carbide memristors with neuromorphic behaviour. By tuning the SiC stoichiometry from Si-rich to near-stoichiometric, distinct synaptic behaviours were achieved for neuromorphic computing. Si-rich SiC devices exhibited volatile, tunable multilevel resistance states under DC and AC bias, enabling the emulation of short-term plasticity (STP), spike-voltage-dependent plasticity (SVDP), and learning–forgetting–relearning processes [2,3]. In contrast, near-stoichiometric SiC devices showed highly linear and programmable long-term plasticity (LTP), with low nonlinearity of 0.08 and uniform conductance updates. Using experimentally extracted device characteristics, artificial neural networks, convolutional neural networks, and reservoir computing systems achieved high pattern-recognition accuracy. All of the above works showed the potential of SiC memristors for neuromorphic computing applications.

Based on these advancements, we now present the first nanoscale SiC-based memristor (schematic shown in Fig. 1a). Decreasing the physical size of the memristors is crucial for making the memristors more compatible with CMOS technology, lowering the area cost and reducing the power consumption. Our device utilizes SiC as the dielectric layer with Cu top electrodes and W bottom electrodes. The width of the interconnect lines of our memristor array is sub-100 nm patterned by e-beam lithography (Fig. 1b). The devices show both volatile and non-volatile switching behaviors by adjusting the compliance current (Fig. 1c and 1d). And they also enable stable and reconfigurable neuronal and synaptic functions such as pair pulse facilitation (PPF), SVDP, spike duration dependent plasticity (SDDP) and LTP shown in Fig. 2. This reconfigurable electrical behaviors of nanoscale Cu/SiC/W memristors takes advantage of simplified hardware design and high density integration for neuromorphic computing.

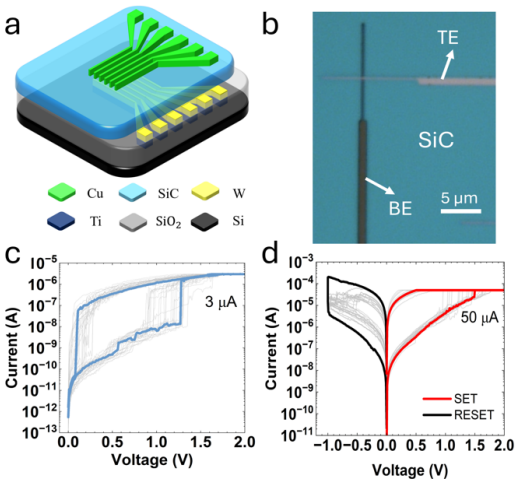


Figure 1. a) The schematic of the nanoscale SiC devices. b) Top view of cross-point SiC devices. c) Volatile switching behavior. d) Non-volatile switching behavior.

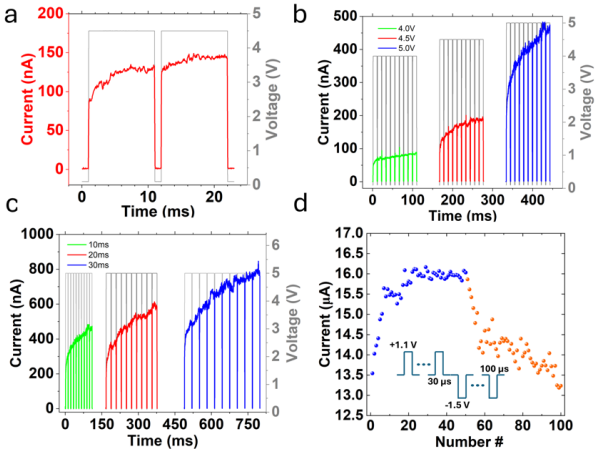


Figure 2. a) The PPF behavior. b) and c) shows the SVDP and SDDP behavior, respectively. d) shows LTP behavior.

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Neural Memristor Rate Model for Compute in Memory Architecture

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Memristor based architectures offer an energy efficient neuromorphic computing by integrating memory and computation within the same physical substrate. Understanding the nonlinear dynamics of memristive devices is essential for exploiting their computational capabilities beyond conventional storage and matrix-vector multiplication. Existing memristor models derive nonlinear behavior from device level switching physics (window functions, thresholds, filament growth, or transport equations) require optimization methods for tuning large no. of parameters. Hence, I propose a simplest neural memristor rate model based on the wilson-cowan framework combined with flux charge state variables to capture emergent computational phenomena such as bistability and Hopf induced oscillations in compute in memory architectures.

Starting from flux charge relationship, the memristor rate model captures the nonlinear conductance evolution of memristive elements. The resulting rate equations establish a direct correspondence between device level memory states and neural population activity, providing a compact framework for analyzing large scale CIM systems. Numerical simulations demonstrate the existence of a supercritical Hopf bifurcation that separates stable fixed point behavior from self sustained oscillatory dynamics. Near the bifurcation boundary, the system exhibits bistability characterized by the coexistence of distinct attractor states, enabling memory retention and state dependent computation. Beyond the critical threshold, stable limit cycle oscillations arise, producing rhythmic activity patterns that can be exploited for temporal information processing and adaptive computation. Phase plane trajectories, bifurcation diagrams, and stability analysis confirm the transition between quiescent, bistable, and oscillatory regimes.

The proposed simplest neural memristor rate model provides a unified theoretical framework linking flux charge memristor physics with neural population dynamics. The results highlight how Hopf bifurcation mechanisms can be harnessed to realize scalable compute in memory architectures capable of both memory storage and oscillatory computation, shifts the focus from device modeling to dynamical computation and system level behavior offering new opportunities for novel design of adaptive and energy efficient neuromorphic hardware.

Novel AgNbO3 thin-film-based threshold-switching devices with an intrinsic Ag source

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Next-generation memory and neuromorphic computing systems require electronic devices with fast switching speed, low power consumption, and excellent scalability. Threshold switching has emerged as a promising candidate because of its volatile resistive switching behaviour and nonlinear current–voltage characteristics, enabling applications in selector devices for high-density memory arrays, neuromorphic computing, and hardware security. In many dielectric systems, threshold switching is commonly associated with an electrochemical metallization process involving the field-driven migration of active metal ions and the formation of conductive metallic filaments. However, most electrochemical metallization-based threshold-switching devices rely on external active metal electrodes or active metal dopants as the source of mobile ions.

In this work, we investigate $AgNbO3_3$ as a novel material system for threshold switching, providing an intrinsic source of mobile Ag ions that facilitates electrochemical switching. Compared with devices that rely solely on Ag injection from an active electrode or dilute Ag dopants, intrinsic Ag in $AgNbO3_3$ enables more controlled and reproducible conductive filament formation, leading to lower operating voltages, improved switching uniformity, and enhanced device stability.

We demonstrate the growth of $AgNbO3_3$ thin films using pulsed laser deposition and confirm their phase using X-ray diffraction. Additional Ag-rich particles distributed through the film provide an intrinsic source of mobile Ag ions for electrochemical switching. Current–voltage (I–V) measurements indicate stable volatile threshold switching with a switching voltage of 1.2 V and a high ON/OFF current ratio of $\sim 10^4$. The role of Ag species in the formation of conductive filaments was analysed, confirming the threshold switching. These findings establish $AgNbO3_3$ as a promising intrinsic Ag-source material for reliable volatile threshold switching and provide a pathway for the development of high-performance selector devices and neuromorphic computing systems.

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Optical Memristors with RGB Sensitivity

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Memristors are attracting growing interest as the rapid expansion of A.I. drives demand for more energy-efficient hardware. Their simple architecture, low power consumption, and tuneable resistive switching properties make them promising candidates for next-generation memory and neuromorphic computing technologies.

Light-sensitive memristors are particularly attractive for neuromorphic vision systems, where they can enable ultrafast image processing within compute-in-sensor and compute-in-memory architectures [1-3]. Zinc sulfide (ZnS) is a wide-bandgap semiconductor that exhibits strong ultraviolet absorption and efficient exciton generation near its band edge, properties that are advantageous for photodetection and light-harvesting applications. Furthermore, its optical and electronic characteristics can be tailored through control of grain size, stoichiometry, and defect density.

In this work, we investigate memristor devices comprising RF-sputtered ZnS thin films sandwiched between indium tin oxide (ITO) top and bottom electrodes. Following an initial electroforming process at 7–8 V, the devices exhibited stable bipolar resistive switching with endurance exceeding 5,000 cycles and highly reproducible current–voltage (I-V) characteristics. The first 100 I-V sweeps of the device after the forming step are shown in Fig. 1.

Optical modulation of the device resistance was examined using an RGB LCD illumination source with the results shown in Fig. 2. Repeatable resistance changes in the range of 10–50 Ω were observed under illumination, with both the magnitude and temporal response dependent on the incident wavelength. In particular, blue light produced a faster response than red light. Devices subjected to electrical stress also displayed distinct optical behaviours, suggesting light-induced processes that may contribute to adaptive or regenerative device functionality.

The observed photoresponse is likely linked to carrier dynamics at the ITO–ZnS interface. Release of trapped electrons may contribute to the conductivity modulation, while photogenerated carriers within the ZnS layer are also expected to play a significant role. The chosen ZnS film thickness appears to provide a favourable balance between optical sensitivity and low-voltage resistive switching, enabling operation within a regime that combines reliable electrical performance with a measurable and repeatable optical response.

These results demonstrate the potential of ZnS-based optoelectronic memristors for multifunctional memory and sensing applications. The findings provide a foundation for future studies aimed at understanding optically assisted resistive switching mechanisms, enhancing photoresponsivity through device engineering, and developing adaptive neuromorphic hardware that integrates memory, sensing, and computation within a single platform.

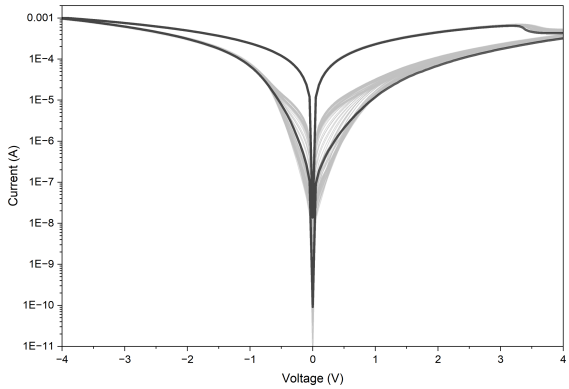


Figure 1. Current–voltage (I–V) characteristics of the 100 sweeps after the forming step.

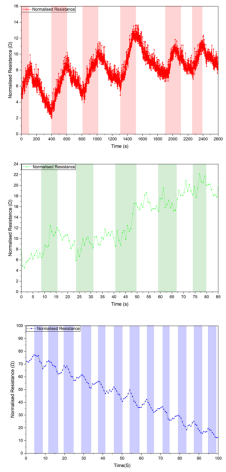


Figure 2. Resistance vs time graphs showing the response of a single device to RGB light. The white band represents the time when the light is off. Red light shown to increase the device resistance, where as blue light decreases it.

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Optically Programmable Ferroelectric Memory with State Dependent Resistive Switching

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Non-volatile memories that can directly interface optical and electronic domains are highly desirable for future communication-linked computing and neuromorphic hardware[1][2]. To explore such functionality in a compact device format, we demonstrate a nanoscale opto-electronic memory based on an epitaxial Ba0.4Sr0.6TiO3 (BST) ferroelectric thin film with a Pt plasmonic resonator that induces localized heating through optical field enhancement (Fig. 1(a) and (c)). The device resistance is programmed by 1550 nm infrared (IR) free-space illumination and subsequently sensed by electrical readout. This approach provides a route toward optically programmable memory devices, where free-space illumination could enable parallel programming of multiple cells while reducing the wiring overhead associated with conventional electrical addressing.

The proposed light-induced switching mechanism is illustrated schematically in Fig. 1(b). The device is first electrically initialized to ON and OFF states by applying positive and negative voltages, respectively. Upon optical excitation, localized heating around the plasmonic resonator raises the local temperature toward the ferroelectric-to-paraelectric transition regime of BST. As the heat dissipates and the temperature decreases, the ferroelectric phase is restored, but the polarization configuration does not fully recover to its original state, resulting in a new remanent resistance state.

Electrical measurements in Fig. 1(d) show reproducible resistance-voltage hysteresis for 50 cycles with low cycle-to-cycle variation and a resistance window of approximately 1-2 orders of magnitude, confirming stable non-volatile switching behavior. More importantly, optical programming produces state-dependent bidirectional resistance evolution. When the device is initialized in the high-resistance OFF state (Fig. 1(e)), successive 1550 nm optical pulses at 16 dBm with 100 ms pulse width gradually decrease the resistance. In contrast, when the device is initialized in the low-resistance ON state (Fig. 1(f)), the same optical stimulus produces a progressive resistance increase. In comparison, repeated electrical read pulses alone cause only minor drift (light blue in Fig. 1(e) and light orange in Fig. 1(f)), confirming non-destructive readout. These results demonstrate a compact BST-based memory device with resistance tuning via IR pulses, providing a promising platform for opto-electronic memory and adaptive computing interfaces.

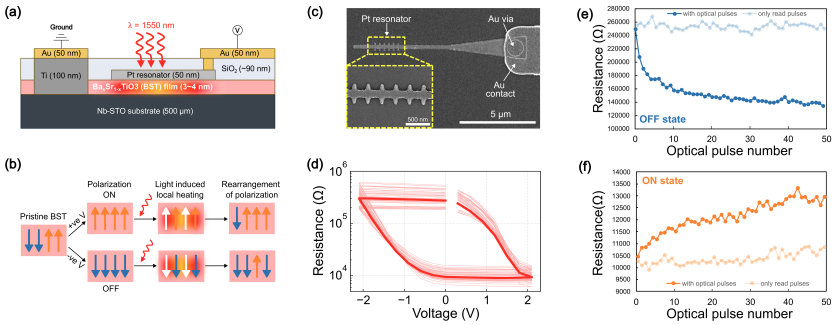


Figure 1. (a) Cross-sectional schematic of the BST device, where the red-colored region indicates the area of localized photothermal heating. (b) Schematic illustration of the proposed light-induced polarization reconfiguration mechanism. (c) SEM image of the device architecture showing the Pt plasmonic resonator (inset) and the Au circular via connected to the top contact electrode. (d) Resistance-voltage hysteresis loop measured for 50 cycles, with the median curve shown in red. (e) Resistance evolution under successive 1550 nm optical pulses with the device initialized in the high-resistance OFF state. (f) Resistance evolution under the same optical stimulus with the device initialized in the low-resistance ON state, confirming bidirectional multilevel programming.

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Oxygen Programmed Memristive Dynamics in Silicon Nanowire Devices for Neural Electronics

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A persistent ambiguity in memristive neural electronics and neuromorphic computing concerns how volatile and non-volatile device behaviors should be related to neural and synaptic functions. Volatile memristive devices are usually linked to transient excitability, whereas non-volatile memristors are used for synaptic conductance memory. In biological neural systems, however, fast dynamics and longer-term state modulation are coupled rather than isolated. Here, we report a quasi-one-dimensional silicon nanowire memristive device whose functional state is programmed by oxygen treatment. This geometry confines charge transport into a narrow silicon pathway, enabling oxygen-programmed device states to be expressed as distinct hysteresis, relaxation, and retention behaviors. By varying the oxygen-related device condition, the platform evolves from weak memory transport to volatile hysteresis and residual conductance memory. These results show that volatility is not only a fixed device label, but a programmable dynamic regime. In this sense, oxygen programming tunes the functional identity of the device across neural and synaptic memristive behavior. Relaxation-dominated states provide neural-like transient responses, while retention-dominated states provide synaptic-like conductance memory. This quasi-one-dimensional silicon platform therefore suggests a route toward adaptive neural electronic devices in which excitability and memory are engineered as coupled physical functions.

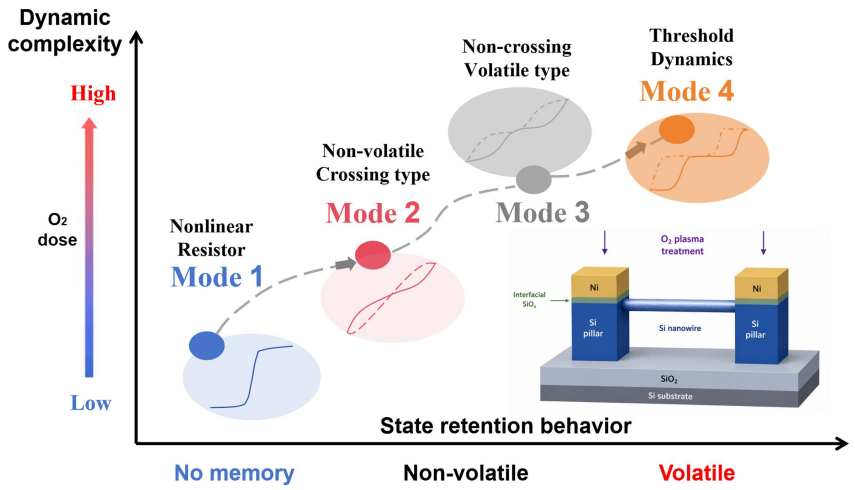


Figure 1. Oxygen programming tunes memristive dynamics across neural- and synaptic-like regimes in a quasi-one-dimensional SiNW platform.

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Phase Transition-Induced Large Memory Window in MoTe2 Ferroelectric Transistor

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Polymorphic MoTe2 provides a unique platform for phase-transition (PT) memristors owing to its reversible switching between semiconducting (2H) and metallic (1T') phases. However, achieving non-volatile phase-transition behavior has remained challenging, as conventional electrolyte gating suffers from volatile characteristics due to mobile ion diffusion. In this work, we demonstrate a non-volatile PT ferroelectric field-effect transistor (PT-FeFET) by integrating a polymorphic MoTe2 channel with a HfZrO2 (HZO) ferroelectric gate insulator. The ferroelectric polarization of HZO drives a robust, electrically-tunable, and long-term non-volatile phase transition in MoTe2. Crucially, the emergence of the 1T' metallic phase circumvents the conventional Vth limitations of standard FeFETs, expanding the memory window across the entire voltage range below the RESET threshold. This results in a superior memory window of 82.5% and a high ON/OFF ratio of 10^6. The device exhibits near-ideal synaptic linearity (β=0.9) and accesses a full spectrum of weights (0-1), leading to an 82% accuracy in CIFAR-10 classification—significantly outperforming conventional FeFET-based systems (59–75%).

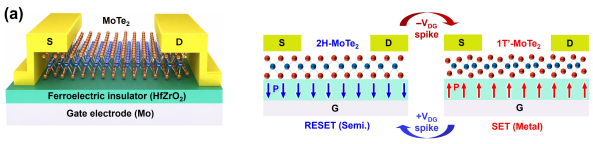


Figure 1. (a) Device structure and polarization-driven phase transition of MoTe2 between semiconducting 2H (OFF) and metallic 1T' (ON) states under VDG spikes.

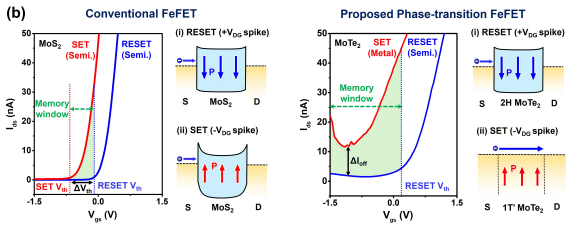


Figure 2. (b) Unlike conventional FeFETs limited by △Vth , the PT-FeFET suppress OFF current and achieves an expanded memory window with enhanced ON/OFF ratio.

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Polarity-Dependent Coexistence of Volatile and Nonvolatile Switching in Ag/a-Si Memristors

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Conductive-bridge random-access memory (CBRAM) has attracted significant interest for neuromorphic computing owing to its simple metal-insulator-metal structure, low operating voltage, and ability to emulate synaptic plasticity [1,2]. Amorphous silicon (a-Si) is a particularly attractive CBRAM switching layer due to its isotropic structure, CMOS back-end-of-line compatibility, and support for Ag filament growth via discrete nanocluster migration [3]. While most CBRAM devices exhibit either volatile or nonvolatile switching, their simultaneous coexistence within a single device — governed intrinsically by polarity — remains rarely reported.

Here we report the polarity-dependent coexistence of volatile and nonvolatile switching within a single bipolar sweep in Ag/a-Si/W CBRAM devices fabricated with a PECVD-deposited a-Si switching layer, Ag top electrode, and W bottom electrode (Fig. 1a). Initial electroforming was carried out under a compliance current (CC) of 1 mA (Fig. 1b). Subsequent bipolar cycling performed with a reduced CC of 200 μA revealed a pronounced polarity asymmetry in the switching characteristics. As shown in Fig. 1c, under forward bias (+V on Ag), the device undergoes an abrupt transition from the high-resistance state (HRS) to the low-resistance state (LRS) at ca. 1.2 V; during the return sweep, the device spontaneously returns to HRS with a hold voltage of ca. 0.2 V, exhibiting volatile threshold switching. In contrast, under reverse bias, the device sets at ca. -0.2 V and subsequently resets at ca. -0.5 V, thereby completing a full nonvolatile unipolar set–reset cycle. This unusual coexistence of volatile and nonvolatile switching modes, governed solely by bias polarity, is highly reproducible over multiple cycles. Interestingly, increasing the CC to 300 μA transforms the switching behaviour into a more conventional bipolar nonvolatile switching, with set under positive bias and reset under negative bias (Fig. 1d).

A tentative mechanism is proposed in Fig. 2. During electroforming, Ag atoms are injected into the a-Si layer to form a conductive filament; the subsequent reset partially ruptures it, leaving a narrow gap (Fig. 2a). Under forward bias at CC = 200 μA, Ag ion migration reconnects the residual filament, which spontaneously dissolves below the hold voltage, yielding volatile switching; under reverse bias, Ag ions are driven by the electric field to reconnect the residual filament, after which localized Joule heating thermally ruptures it, completing a nonvolatile set-reset cycle within the same sweep (Fig. 2b). At CC = 300 μA, the higher compliance current produces a more robust filament, resulting in bipolar nonvolatile switching (Fig. 2c). This polarity-governed coexistence of volatile and nonvolatile switching highlights the potential for neuromorphic hardware implementing both short-term and long-term plasticity.

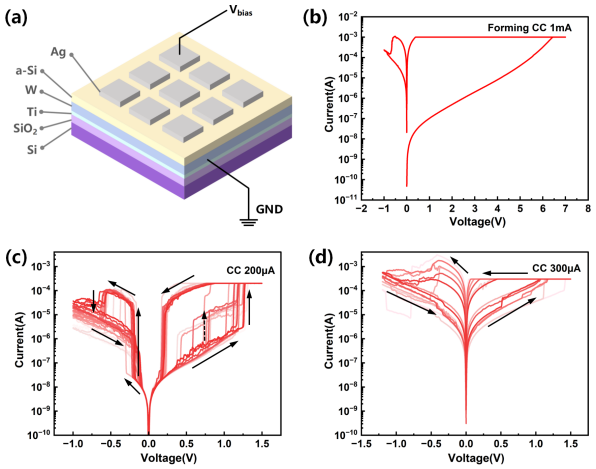


Figure 1. (a) Ag/a-Si/W memristor structure. (b) Electroforming characteristics. (c) Polarity-dependent coexistence of volatile and nonvolatile switching. (d) Bipolar nonvolatile switching.

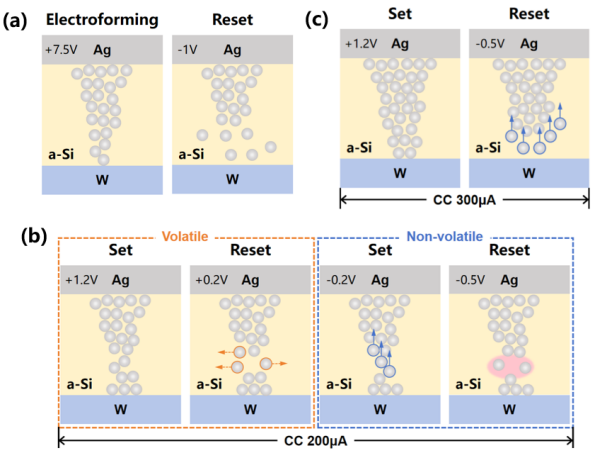


Figure 2. Proposed switching mechanisms in Ag/a-Si/W CBRAM devices: (a) electroforming; (b) volatile switching and nonvolatile switching at CC = 200 μA; (b) bipolar nonvolatile switching at CC = 300 μA.

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QSPICE simulation of memristive devices using the dynamic memdiode model

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Memristive devices have attracted considerable interest for applications in non-volatile memory, neuromorphic computing, and unconventional information processing due to their nonlinear dynamics and history-dependent resistive states. Reliable and computationally efficient simulation tools are therefore essential for the analysis and design of circuits and networks incorporating such devices.

This work presents the implementation and evaluation of a memristor compact model in QSPICE [1], the next-generation circuit simulator introduced by Qorvo in 2023 and developed as the successor to LTspice. The model is based on the dynamic memdiode framework [2], a physics- and behavior-inspired compact formulation capable of reproducing resistive switching phenomena across a wide range of memristive technologies while remaining compatible with SPICE-based environments . The transition from LTspice to QSPICE is motivated by improved numerical performance, enhanced computational efficiency, extended behavioral modeling capabilities, and native support for C++-based extensions.

Three memdiode model variants with increasing complexity are analyzed. The first level corresponds to a minimal implementation designed for efficient large-scale simulations and conceptual studies, capturing the essential hysteretic switching behavior with a reduced parameter set. The second level extends this formulation by introducing additional degrees of freedom that improve the description of progressive reset dynamics. The third level incorporates abrupt switching transitions, accounting for snapback and snapforward phenomena commonly observed in filamentary resistive switching devices, thereby improving the representation of highly nonlinear state evolution. The proposed model variants are validated against experimental measurements obtained from HfO_2-based memristive devices fabricated at TUDa [3]. See Figs. 1 and 2.

Performance is evaluated in terms of numerical stability, computational cost, and accuracy in reproducing key experimental signatures, including current–voltage hysteresis loops and state evolution under voltage-driven operation. Results show that QSPICE provides a robust framework for memristor compact modeling, preserving the familiar LTspice workflow while extending flexibility for advanced behavioral implementations. The comparative analysis highlights the trade-off between computational efficiency and physical fidelity, providing practical guidelines for model selection depending on the target application, ranging from large-scale circuit simulations to detailed device-level analysis.

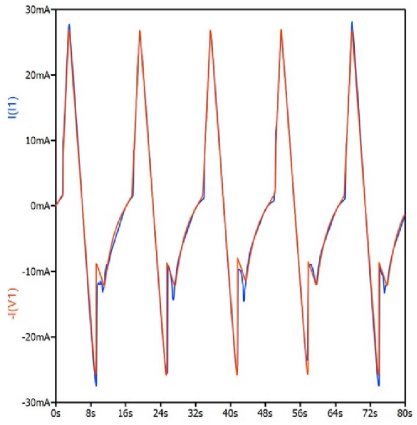


Figure 1. Current-time characteristics. Experimental (blue line) and model (red line) results using the memdiode model.

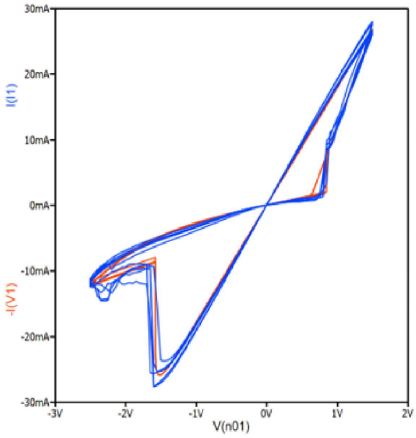


Figure 2. Current-voltage characteristics. Experimental (blue line) and model (red line) results using the memdiode model.

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Quantum theory of diffusive memristors

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We develop a comprehensive theoretical framework for diffusive memristors, whose operation relies on the formation and disruption of conducting filaments (CFs) comprised of metallic (Ag) ions bridging electrodes sandwiching dielectric (amorphous silicon). It is based on a stochastic model of CF formation and disruption. To describe conductive properties of the filaments and (non-metallic) temperature-dependence of memristor resistivity, observed in experiments, we apply quantum Lifshitz-Kirpichenkov theory–the quantitative generalization of the trap-assisted-tunneling model [1]. We investigate working regimes of memristors including current–voltage characteristic and resistance modulation by SET and RESET impulses. The theoretical model achieves qualitative and semi-quantitative agreement with previously reported experimental results for both I-V characteristics and conductivity temperature dependence. The framework further enables prediction of switching thresholds and resistance window as functions of device geometry and material properties, providing a physically grounded design tool for memristor optimization.

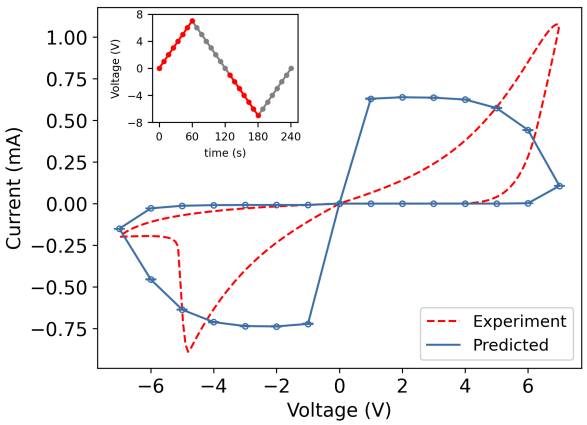


Figure 1. Current–voltage characteristics of the memristor predicted by the proposed model [2] and experimental [3].

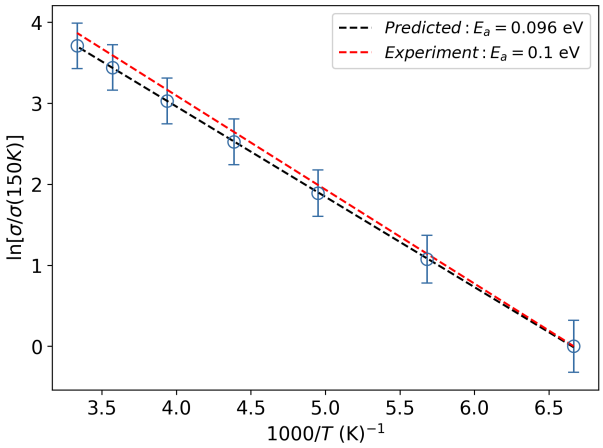


Figure 2. Temperature dependence of the conductivity relative to its value at 150 K, as a function of 1000/T .

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Reconfigurable Threshold in NbTex Selector-Only Memory for Artificial Neurons

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In biological nervous systems, neurons serve as the fundamental units for receiving, integrating, and transmitting information through spike-based activity. The dynamic regulation of neuronal excitability underlies both intensity coding and temporal coding. However, existing neuromorphic hardware is usually limited by device functionality and has difficulty reproducing, at the device level, the rich characteristics of biological neurons, namely threshold activation and state tunability. This limitation constrains the integration capability of advanced bioinspired functions. The concept of selector-only memory (SOM), which uses threshold characteristics as the storage medium, provides a new device basis for realizing storable and tunable neuronal excitability. In this work, we propose an analog SOM device based on NbTex. By exploiting the ovonic threshold switching characteristics of amorphous telluride and the modulation of Te-related defect states, the device realizes stable threshold switching and multilevel tunable threshold states. The device exhibits fast threshold switching, good cycling stability, and timescale-dependent threshold evolution. Conductive mechanism analysis indicates that the threshold modulation mainly originates from changes in trap activation energy. Furthermore, based on this neuron-like threshold device, we realize two key neural functions, namely intensity modulation and timing control, which can be applied to excitability-tunable neurons and spinal-reflex-inspired multi-muscle systems. This artificial neuron device and readout paradigm, centered on programmable threshold states, provide a new implementation pathway for constructing neuromorphic hardware with intrinsic plasticity and timing regulation capabilities.

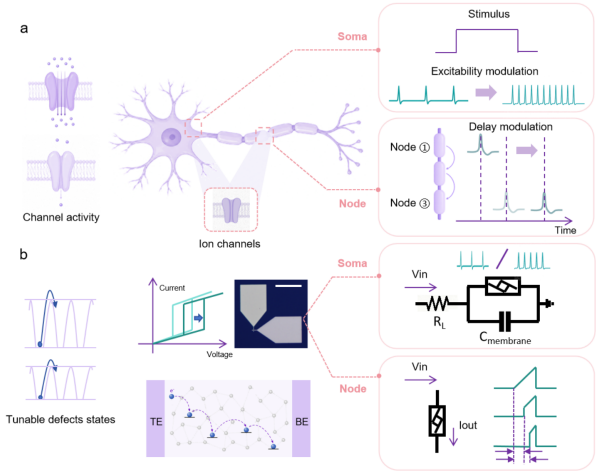


Figure 1. Bioinspired concept of programmable $NbTe_x$ selector-only memory as an artificial ion channel.(a) Biological ion channels(b) Schematic illustration of the $NbTe_x$ selector-only memory device and its functional mapping to artificial ion channels.

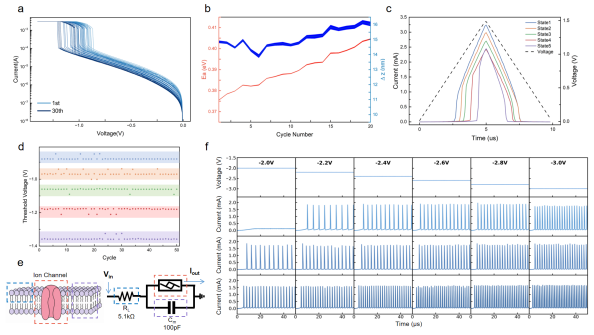


Figure 2. Programmable threshold states and neuromorphic functions of the $NbTe_x$ device.(a) Evolution of threshold switching characteristics during repeated electrical stimulation, showing gradual modulation of the threshold state and subthreshold conductance.(b) Extracted fitting parameters based on the thermally assisted hopping model.(c) Dynamic triangular-wave readout of multiple programmed threshold states, where different threshold states are converted into distinct triggering times and output current responses.(d) Cycling readout stability of multiple threshold states.(e) Schematic of the artificial ion-channel neuron circuit, in which the $NbTe_x$ device acts as a threshold-triggered channel element and modulates membrane-capacitor discharge dynamics.(f) Output spiking responses of the artificial neuron under different input voltages and programmed threshold states.

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Simulation of field-dependent conductivity in AlOx/PCMO memristive devices

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Area-dependent resistive switching in PCMO-based memristive devices is driven by the electric-field-induced movement of oxygen vacancies between the PCMO and a tunnel oxide [1]. Understanding the electric-field distribution across the device stack is therefore essential for explaining how switching behavior depends on PCMO and oxide thickness.

Continuum simulations are employed to investigate the electric-field distribution in AlOx/PCMO memristive heterostructures. The model incorporates a non-linear, field-dependent conductivity for both AlOx and PCMO, motivated by ion-hopping transport [1]. The electric-field distribution is obtained by solving the coupled current-continuity and electrostatic equations.

Three device configurations — polycrystalline (c-PCMO), quasi-amorphous (qa-PCMO), and amorphous (a-PCMO) — with varying AlOx thicknesses are analyzed. Simulations fitted to experimental data reveal that the voltage drop across the AlOx layer strongly modulates the field available for oxygen-vacancy migration in the PCMO. Depending on stack configuration, increasing AlOx thickness can either enhance or suppress the local electric field, producing significant variations in ON/OFF ratio. The simulated field distributions reproduce the experimentally observed switching trends and account for the absence of switching in specific thickness ranges through insufficient field strength for vacancy transport.

These results demonstrate that the electric-field distribution within the tunneling oxide is one of the key factors governing oxygen-vacancy dynamics and, consequently, area-dependent switching characteristics in AlOx/PCMO devices. The findings provide design guidelines for optimizing oxide thickness and device architecture toward improved memristive switching performance.

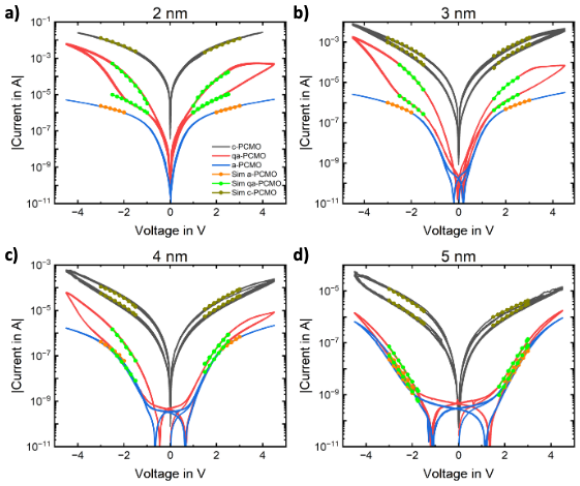


Figure 1. Fitted I–V characteristics using the field-dependent conductivity model.

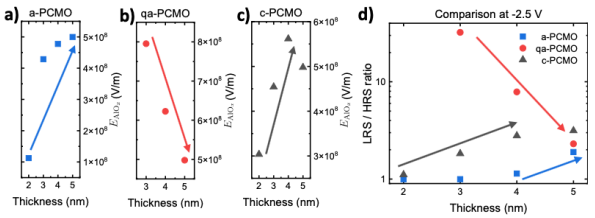


Figure 2. Correlation between the electric field in AlOx at -2.5 V in the HRS of a) a-PCMO, b) qa-PCMO, and c) c-PCMO devices as a function of AlOx thickness and the ON/OFF ratio d) after the SET read out at -2.5 V. Arrows were used to visually highlight this correlation

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SPICE Building Block for Temperature-Sensitive Analogue Memristors Using Hybrid Physical-Compact Modelling

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With the increasing demand for data processing, conventional computing architectures struggle to keep up. Concepts such as in-sensor and in-memory computing aim to overcome the Von Neumann barrier by processing data directly at the sensor level, reducing data movement and enabling low-latency operation [1, 2]. Analogue interface-type memristors are highly promising for this paradigm, potentially serving as both computational nodes and environmental sensors [3].

In this work, we develop a hybrid physical-compact temperature model to evaluate the viability of analogue memristors fabricated at the Institute of Electrical Engineering of the Slovak Academy of Sciences (IEE SAS) as temperature sensors. Devices were measured in temperatures ranging from 30°C to 150°C. To acquire the necessary data, an automated measurement system was implemented using an Agilent E5363A SMU, a Keithley 7001 multiplexer, and a Temptronics TP3000 heating system. This setup enabled repeatable, high-throughput characterisation across multiple devices within a single thermal cycle. Using this system, measurement variability caused by probe repositioning was also significantly reduced.

Multiple thermally activated conduction mechanisms for wide-bandgap dielectrics were compared to model the temperature-dependent behaviour in a single resistive state. Initial measurements indicated the Poole- Frenkel (P-F) effect as the dominant mechanism. Further analysis revealed a linear relationship between the prefactor and the activation energy. This behaviour is consistent with the Meyer-Neldel rule (MNR), indicating a compensation process that influences the P-F effect [4].

Consequently, an empirical, voltage-dependent model combining P-F emission with MNR-type compensation behaviour is proposed. The model reproduces the measured temperature dependence with high agreement. Using this model, a SPICE-compatible building block has been implemented. This hybrid physical-compact representation allows for practical circuit-level simulations, providing a foundation for future integration into thermal in-sensor computing arrays.

Funded by the EU NextGenerationEU through the Recovery and Resilience Plan for Slovakia under the project No. 09I02-03-V01-00038 (Stephanik), and by the M-ERA.net project PhotoPrint.

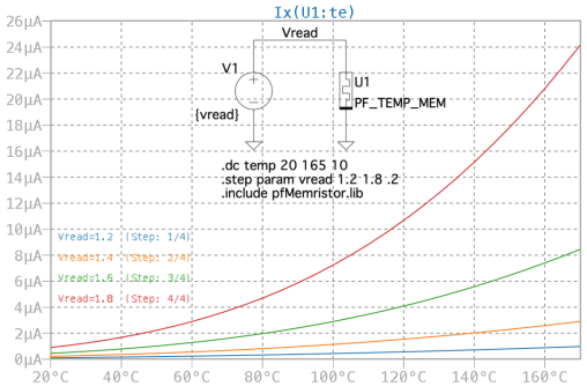


Figure 1. I-T characteristic of simulated memristive device from SPICE simulation

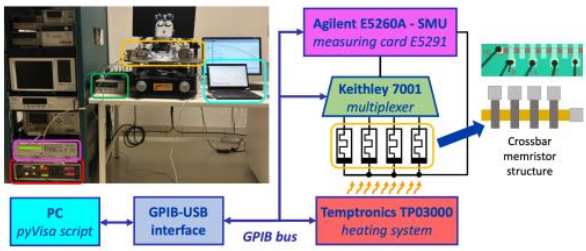


Figure 2. Block diagram of automated measurement system for temperature characterisation

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Switching Behavior of FCM-Based Ohmic Memristors under Various Electrical Conditions

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Resistive random-access memory (ReRAM) devices have attracted considerable attention as promising candidates for next-generation non-volatile memory owing to their low-power operation, scalability, and potential for neuromorphic computing. Among them, filament conductivity change mechanism (FCM)-based ohmic memristors exhibit stable analog switching, high thermal stability, and good endurance. In this work, the electrical switching characteristics of ohmic memristors were investigated through I–V measurements under various current compliance levels and voltage sweep ranges. Pulse measurements were also performed to examine the device behavior under voltage pulses. These results provide a better understanding of the switching behavior of ohmic memristors under various electrical conditions.

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Toward Synaptic Compact Modeling of an Ultra-Low-Voltage Ag/WTe_2 CBRAM with Multi-Timescale Forgetting for Future Lifelong Learning Computing

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Edge artificial intelligence (AI) demands computing systems with high energy efficiency, local learning capability, and scalability, which are difficult to achieve using the conventional von Neumann architecture[1,2]. Inspired by the human brain, neuromorphic computing employs spike-based Hebbian learning governed by spike-timing-dependent plasticity (STDP) to enable local weight updates, offering a promising approach for energy-efficient and lifelong learning systems[3,4]. In such systems, artificial synapses are fundamental building blocks responsible for information storage, learning, and recognition[5]. Among emerging synaptic devices, resistive random-access memory (RRAM) and conductive-bridge random-access memory (CBRAM) have attracted considerable attention owing to their analog resistive switching behavior governed by conductive filament dynamics, making them well suited for emulating complex biological synaptic functions[6]. To evaluate the performance of the electronic synapse when implemented on an analog spiking circuit, the development of a synapse compact model is necessary to integrate within circuit-level simulations. However, current compact models of RRAM and CBRAM focus primarily on reproducing direct-current (DC) switching characteristics, which cannot thoroughly capture the dynamical nature of input- and state-dependent forgetting behavior of synapse. In this work, Ag/WTe2 CBRAM is fabricated using Radio-Frequency (RF) sputtering and e-beam evaporation, and the experimental results are used as the basis for synaptic compact model development. Fig. 1 illustrates that Ag/WTe2 CBRAM exhibits analog RS at an ultralow operating voltage of 0.3 V in the DC sweep test and demonstrates typical synaptic properties, including long-term potentiation (LTP), long-term depression (LTD), pair-pulse facilitation (PPF) with spiking rate-dependent plasticity (SRDP), and multi-timescale relaxation of excitatory postsynaptic current (EPSC), laying the foundation for further investigation of synaptic behavior. These findings provide a foundation for modeling power-law forgetting and cascade-memory behavior associated with continual learning and memory consolidation[7]. In the simulation work, by optimizing the parameters in the RRAM compact model proposed by Jiang et al. in 2016[8], the simulated I-V curve matches the DC sweep experimental result well, and the simulated potentiation response under various pulse conditions are demonstrated (Fig. 2). In addition, the algorithm of the compact model can be improved to capture essential synaptic plasticity. In conclusion, this work demonstrates synaptic plasticity and multi-timescale forgetting properties in the Ag/WTe2 CBRAM at ultralow operating voltage and highlights the necessity of developing compact models capable of reproducing synaptic plasticity for practical neuromorphic processors.

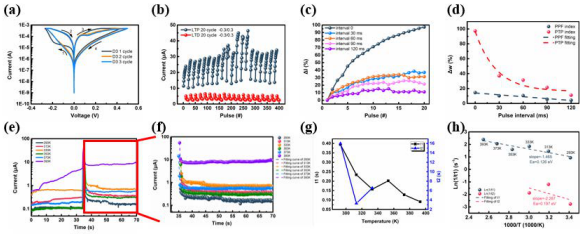


Figure 1. (a)DC sweep (b)LTP and LTD (c)SRDP (d) PPF and PTP (e)I-t curve of STP test under different temperatures (f)EPSC under different temperatures (g)decay time constant of fitting read curve under different temperatures (h) activation energy fitted by Arrhenius relation

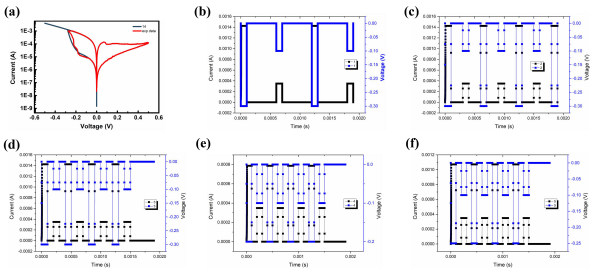


Figure 2. (a)I-V curve of simulation (black) and experiment (red). simulation of pulse response with (b) -0.3 V SET, -0.1 V read, width 0.1ms, interval 0.5 ms (c)-0.3 V SET, -0.1 V read, width 0.1ms, interval 0.2 ms (d) -0.3 V SET, -0.1 V read, width 0.1ms, interval 0.1 ms (e) -0.2 V SET, -0.1 V read, width 0.1ms, interval 0.1 ms (f) -0.25 V SET, -0.1 V read, width 0.1ms, interval 0.1 ms

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Ultra-low Power Memristive Switching through Electro-Thermally Induced Conductive Channels in VO_2 Thin Films

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Memristive devices based on correlated oxide materials are attracting significant interest for next-generation non-volatile memory and neuromorphic computing owing to their scalability, low energy consumption, and tunable resistance states. In this work, we demonstrate resistive switching in VO_2 thin film memristors fabricated on SiO_2 (300 nm)/Si substrates showcasing its compatibility with established CMOS fabrication processes, offering a viable pathway toward large-scale integration of memristive technologies. Application of a 14 V bias induces localized Joule heating, triggering the formation of a conductive channel within the VO_2 layer and enabling stable resistive switching. The resulting device exhibits a large resistance window with a ROFF/RON ratio exceeding 10^3, ensuring clear distinction between memory states and reliable device operation. Electrical measurements reveal that conductive channel formation occurs at a power of 224 mW, corresponding to the thermally driven phase transition in VO_2. Remarkably, once the channel is established, the memristor operates at an ultralow voltage below 500 µV at an expense of only 100 pW. This combination of low operating voltage and picowatt-level power consumption represents a substantial step toward energy-efficient memory and computing hardware. These findings provide new insights into the switching dynamics of VO_2 thin films and establish a foundation for the development of energy-efficient electronic and cognitive computing systems.

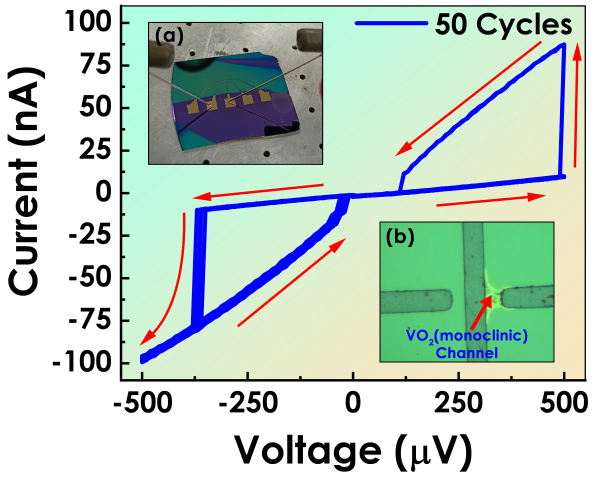


Figure 1. I-V characteristic obtained for 50 cycles, inset (a) shows the probed device and (b) shows the VO_2(monoclinic) channel formed across two Au contact.

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Vertical Nanoporous Silica Memristors with Electrode-Dependent Switching Dynamics

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Memristive devices are promising candidates for neuromorphic and memory electronics due to their tunable resistive switching dynamics [1,2]. Nanoporous materials are attractive active layers because their high surface-to-volume ratios, efficient electron transport, and controllable pore geometries enable precise regulation of ion migration and nanoscale switching functionality [3].

In this work, we investigate memristors based on vertically structured nanoporous silica ($nSiO_2$) films fabricated by electrochemically assisted self-assembly (EASA). The synthesis process, vertically aligned nanochannel structure, and device configurations are illustrated in Fig. 1a–c. The highly ordered vertical nanopores provide confined pathways for ion transport and conductive filament evolution, enabling controllable resistive switching behaviour.

By employing different active electrode materials, the devices exhibit distinct switching characteristics associated with electrode-dependent filament dynamics. Silver-based devices exhibit both volatile and non-volatile switching behaviour, whereas copper-based devices show comparatively stable non-volatile resistive switching under the same operating conditions (Fig. 2a–d). These results highlight the strong influence of active electrode materials on filament stability and relaxation processes in vertically structured nanoporous architectures.

Building upon these complementary properties, we further propose a hybrid Ag/Cu memristive architecture for neuromorphic computing, as schematically illustrated in Fig. 2e. In this approach, Ag-based devices exploit their intrinsic short-term plasticity (STP) and dynamic switching behaviour to function as a physical reservoir, while Cu-based devices provide stable long-term plasticity (LTP) for synaptic weight storage and learning. The hybrid system is evaluated on both MNIST and Fashion-MNIST classification tasks, demonstrating the advantages of integrating volatile and non-volatile memristive functionalities within a unified neuromorphic framework.

To further understand the distinct switching dynamics of Ag- and Cu-based devices, we also develop a cluster-based modelling framework that provides physical insight into the influence of active electrode materials on conductive filament evolution in vertically structured nanoporous memristors. This work demonstrates the potential of vertical nanoporous silica memristors as a versatile platform for tunable neuromorphic and memory technologies, spanning dynamic reservoir computing and stable non-volatile in-memory learning systems.

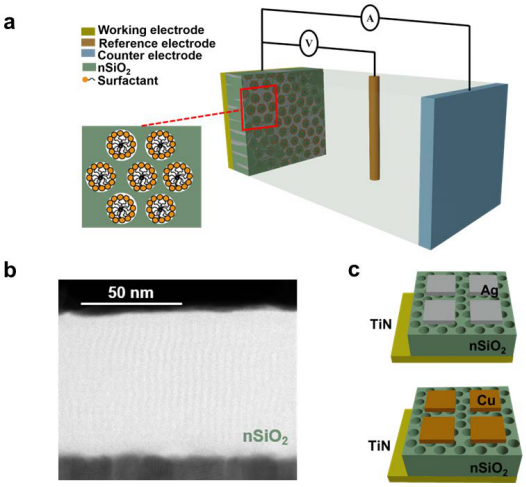


Figure 1. (a) Schematic illustration of the fabrication of the vertically aligned nanoporous silica ($nSiO_2$) film via the electrochemically assisted self-assembly (EASA) method. (b) Cross-sectional TEM image of the $nSiO_2$ film, showing the well-defined vertically aligned porous channels. (c) Schematic representations of the $Ag/nSiO_2$ and $Cu/nSiO_2$ memristor device structures.

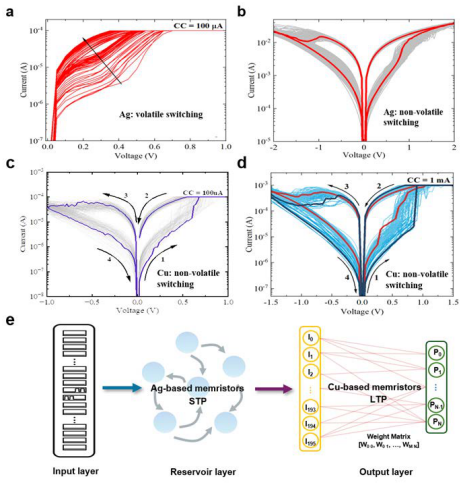


Figure 2. (a) Representative volatile switching behaviour of the $Ag/nSiO_2$ device operated under a compliance current of 100 µA. (b) Representative non-volatile switching behaviour of the $Ag/nSiO_2$ device. (c) Representative non-volatile switching behaviour of the $Cu/nSiO_2$ device operated under a compliance current of 100 µA. (d) Representative non-volatile switching behaviour of the $Cu/nSiO_2$ device operated under a compliance current of 1 mA. (e) Schematic illustration of the proposed hybrid Ag/Cu memristive architecture for neuromorphic computing

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Volatile memristive devices with tunable temporal dynamics for event-based sensing

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Volatile memristive devices with tunable decay dynamics could support a range of neural-inspired tasks and efficient signal processing, for neuromorphic computing [1] and edge computing applications [2], respectively. Their versatility could enable the same device to be employed across diverse temporal coding, sensing, and learning applications in adaptive edge-computing scenarios, while preserving low circuit complexity. Area-dependent volatile devices, in particular, exhibit gradual switching and low variability, enabling stable multistate operation. However, achieving controllable and reproducible temporal responses and establishing a clear physical understanding of the mechanisms governing volatility remain key challenges for their practical implementation. Here, we demonstrate a BEOL CMOS-compatible area-dependent amorphous $SrTiO_3$ (a-STO)-based memristive device with tunable volatile dynamics, in which the characteristic relaxation timescales can be systematically controlled over a broad range, from milliseconds to tens of seconds. Through a combination of experimental investigations and physical analysis, we elucidate the mechanisms governing the observed temporal behavior and identify multiple pathways for tuning device volatility via both stimulus conditions and stack engineering. Furthermore, we conduct a comprehensive study on the reliability of the device and its capability for multilevel operation. Finally, we demonstrate its applicability for event-based sensing by using its volatile dynamics to encode the temporal separation between asynchronous events, highlighting its suitability for memristive TDE [3] architectures with tunable temporal sensitivity.

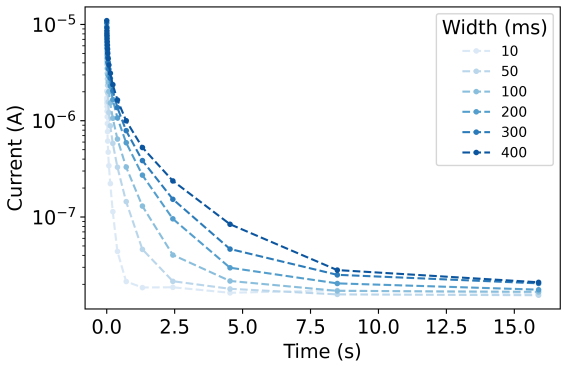


Figure 1. Current decays from 20nm thick a-STO devices after 6.0 V SET pulses with varying width between 10 and 500 ms.

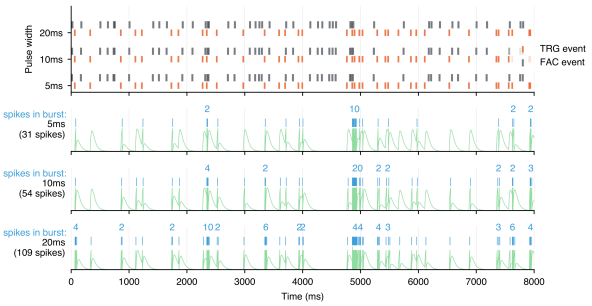


Figure 2. The use of the device as a circuit element to encode the spatiotemporal correlation of events from an event based camera. The tunable volatility is exploited to achieve sensitivity for longer time intervals between TRG and FAC events, enabling tunable temporal sensitivity.

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Posters

Material Processing

A Single-Stack $LaVO_3$ Memristor for Brain-Inspired Learning and Hardware- Level Encryption

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Oxide memristors capable of simultaneously enabling neuromorphic computing and hardware security are highly desirable for next-generation intelligent electronics. Here, we demonstrate an Ag/LaVO3/ITO memristor fabricated by pulsed laser deposition, exhibiting stable bipolar resistive switching governed by oxygen-vacancy filament formation and rupture through a valence-change mechanism. The device reproduces key synaptic functions, including short-term plasticity, long-term potentiation/depression, and spike-rate-dependent plasticity on millisecond timescales. Experimentally measured conductance states were mapped to synaptic weights in an ex-situ artificial neural network, achieving 94% recognition accuracy on the MNIST handwritten digit dataset with software-comparable performance. Beyond neuromorphic computing, the intrinsic stochasticity of filamentary switching serves as a robust entropy source for hardware cryptographic key generation, enabling secure image encryption and decryption. The device further demonstrates excellent long-term stability, retaining a stable memory window for over 450 days under ambient conditions, highlighting its reliability for practical applications. By integrating memory, learning, and hardware security within a single perovskite oxide stack, the $LaVO_3$ memristor demonstrates the potential of multifunctional memristive devices for future in-memory computing and secure edge intelligence.

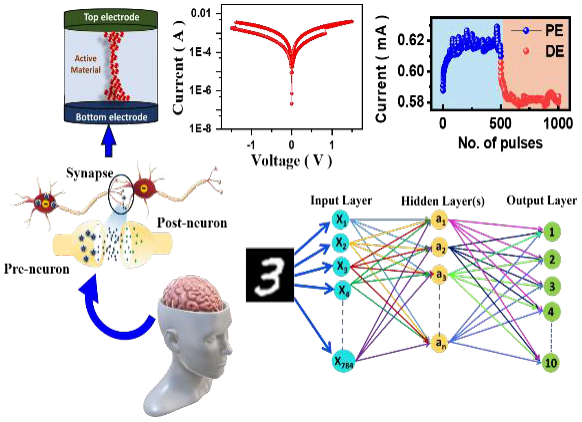


Figure 1. Graphical abstract illustrating Ag/$LaVO_3$/ITO memristor enabling neuromorphic digit recognition

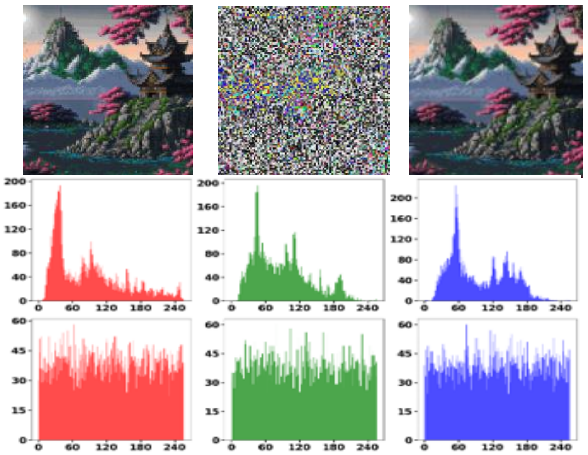


Figure 2. Hardware-level image encryption and decryption generating noise-pattern ciphertexts with restored RGB histograms, driven by filament-stochasticity of the same device.

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A study on materials of ECRAM devices for neuromorphic computing

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The rapid growth of artificial intelligence and machine learning workloads has exposed critical limitations of conventional von Neumann computing architectures, where the physical separation of memory and processing units creates a substantial energy and latency bottleneck. Neuromorphic and in-memory computing paradigms have emerged as promising alternatives, enabling massively parallel analog computation directly within the memory array.

Among the candidate synaptic devices, electrochemical random-access memories (ECRAMs) based on oxygen-ion migration stand out for their gradual and reproducible conductance modulation, high linearity, and device-to-device uniformity, properties essential for accurate analog weight updates in hardware neural networks. [1]

Despite the remarkable results in fabrication (recently an array of 4096 ECRAM devices was demonstrated [2]), physical mechanisms remain highly debated in the community, leaving a gap between the electrical behaviour of ECRAM and the physical properties of the materials employed in the devices.

With this in mind, we developed an ECRAM with a WO3-x channel, HfO2 electrolyte and WO3-x reservoir (Fig. 1a). In principle, applying a positive (negative) voltage to the gate terminal, oxygen vacancies are inserted (removed) from the channel, leading to a non-volatile variation of its conductance.

Conversely to other studies, in which metal-oxides were deposited using sputtering, we fabricated ECRAMs using electron beam evaporation for the WO3-x layers. For the HfO2 electrolyte we tested both atomic layer deposition (ALD) and e-beam evaporation. As confirmed by X-ray reflectivity (XRR) and spectroscopic ellipsometry (SE), the density of WO3 and HfO2 thin films deposited using e-beam evaporation is significantly lower compared to the values reported for crystalline oxides, as well as amorphous HfO2 deposited by ALD, and we are interested in studying the effect of the porosity of the materials on the electrical behaviour. Oxides deposited by electron beam evaporation could impact on the ionic conductivity of the electrolyte or enhance the diffusivity of oxygen vacancy into the WO3-x channel, compared to films deposited via sputtering or other techniques. The channel oxide was crystallized with an annealing at 450°C for 30 s in N2 atmosphere, to enhance electrical conductivity; a comparison of the surface morphology is reported in Fig. 1b. Characterization of the devices also included XPS and ToF-SIMS depth profiling, to assess chemical composition, and X-ray diffraction (XRD) to study crystallinity.

The electrical behaviour was studied both in quasi-static regime (DC) and in pulsed regime, obtaining performances comparable to other oxygen-based ECRAMs reported in literature. Figs. 2a and 2b show the drain-source and gate-source current of a device sweeping the potential at the gate in quasi-static regime. A difference of 3 order of magnitude in LRS and HRS was measured for the I_DS, while I_GS shows a peak associated with redox reactions. We further investigated those reactions with cyclic voltammetry measurements. Deepening the comprehension of those mechanisms is fundamental to better understand the link between physical properties and electrical behaviour of the devices, paving the way to a more aware and precise engineering of materials.

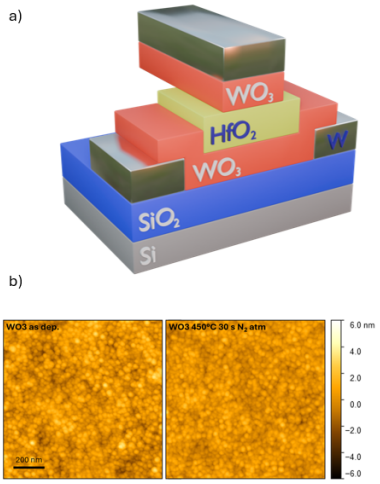


Figure 1. a) Schematic of the ECRAM stack deposited by e-beam evaporation. From the bottom: Si with 50 nm thermal SiO2 substrate, 20 nm thick WO3 channel, 50 nm HfO2 electrolyte, 30 nm WO3 reservoir; source, drain and gate contacts are 30 nm thick W. b) AFM image of the surface of amorphous WO3 deposited using e-beam evaporation (left) and crystalline WO3 after annealing (right).

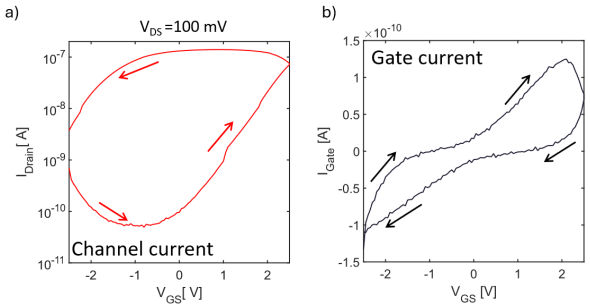


Figure 2. a) Drain-source current applying a triangular sweep to the gate. b) Gate current hysteresis.

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Analysis of Ion Energy Barrier Modulation and Enhanced Memristive Effects through Fluorine Doping for Memristive Neuromorphic Systems

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The exponential growth of artificial intelligence (AI) computations has generated a notable demand for computing solutions that offer low power consumption and high parallelism. Among the various alternatives to conventional system architectures, memristor-based computing systems have garnered considerable attention. However, the inherent instability in memristor operation due to stochastic ion movements poses a significant challenge, impeding the further advancement of memristive computing systems as commercially viable AI tools. Here, we propose an innovative method to address the reliability issues associated with memristors and enhance device performance by introducing fluorides into the switching layer. Our experiments demonstrate enhanced switching windows, reduced device variations, and improved switching speeds through the strategic addition of fluorine into dynamic TiOx memristors (Fig. 1). Furthermore, atomistic simulations elucidate how fluorides attract oxygen vacancies, thereby improving reversible redistribution and uniformity (Fig. 2). Migration barrier calculations indicate that fluorides also decrease the migration energies of nearby oxygen vacancies, resulting in accelerated switching speeds. Additionally, Voronoi volume analysis reveals principles into the electrostatic repulsion of migrating species. Collectively, these findings establish a promising methodology and principles for developing reliable memristors, contributing to the advancement of hardware-based AI systems in the future.

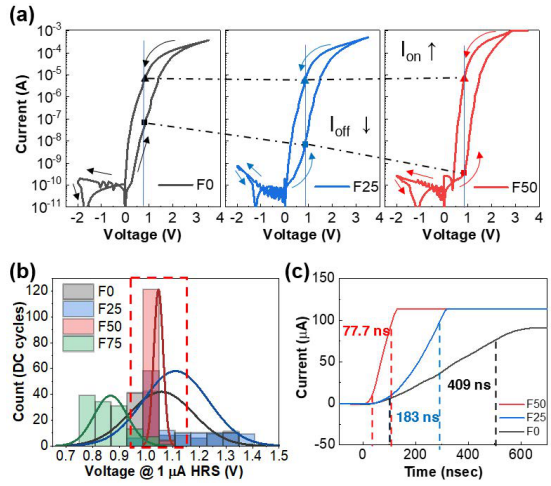


Figure 1. Experimental demonstration of (a) enhanced switching window, (b) reduced device variations, and (c) improved switching speeds through fluorine incorporation.

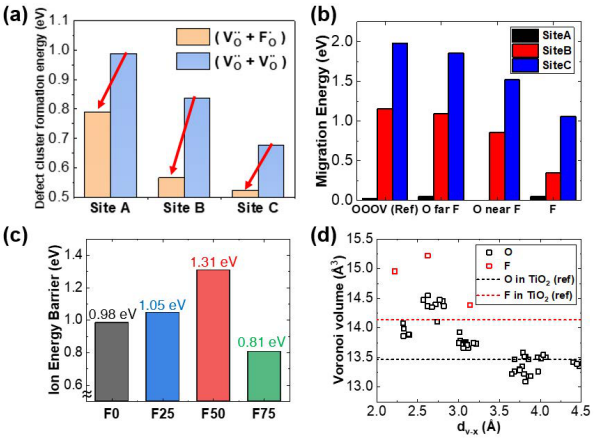


Figure 2. Atomistic simulation results of (a) reduced cluster energy, (b) lowered migration energy, (c) increased ion energy barrier, and increased Voronoi volume by fluorine.

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Band-engineering in area-dependent IGZO-based memristive devices

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Redox-based resistive switching random access memory (ReRAM) devices are widely investigated as promising building blocks for emerging computing paradigms, including neuromorphic computing and computing-in-memory [1-3]. Among the various ReRAM implementations, area-dependent devices operating via the valence change mechanism (VCM) are particularly attractive because they exhibit intrinsic analog switching behavior and reduced device-to-device and cycle-to-cycle variability [4], [5]. In these devices, both the high-resistance state (HRS) and low-resistance state (LRS) scale with device area, indicating that resistive switching is distributed across the entire device area, which inherently suppresses localized stochastic effects and thereby enables low device-to-device and cycle-to-cycle variability as well as gradual, analog switching behavior [6].

IGZO-based area-dependent memristive devices are particularly promising due to the room-temperature deposition of amorphous IGZO in a fully CMOS BEOL–compatible process. In addition to their compatibility with advanced integrated circuits, they show strong potential for flexible electronics [7] and photosensing applications [8]. Nevertheless, the physical mechanisms governing resistive switching and the role of individual interfaces in complex oxide heterostructures remain insufficiently understood, limiting the rational design and optimization of memristive devices.

In this work, we establish and experimentally validate a methodology for understanding and engineering area-dependent IGZO-based memristive devices through quantitative energy-band analysis. Numerical simulations of the energy-band alignment, electric-field distribution, and current densities are employed to identify the dominant switching interface and predict device characteristics. As a proof of concept, W/WO_x/IGZO/top-electrode (TE) device stacks with different TE materials are fabricated and electrically characterized. The resulting devices exhibit gradual, synaptic-like plasticity and area-dependent switching behavior. By varying the top electrode, the switching polarity, current levels, and overall device characteristics can be systematically tuned. The experimentally observed electrical behavior is consistently explained by the simulated band structures, revealing how interface-dependent band alignment governs resistive switching.

To experimentally verify the proposed design framework, in situ XPS band-alignment measurements are performed at both the WO_x/IGZO and IGZO/Pt interfaces. The experimentally extracted band offsets and band-bending profiles show good agreement with the simulations, providing independent validation of the predicted energy-band structure. Based on the resulting band diagrams, the measured current–voltage characteristics are quantitatively described using the Tsu–Esaki tunneling model while accounting for quasi-Fermi-level distributions. The obtained fits are consistent with both the XPS measurements and literature values. This comprehensive energy-band analysis provides a powerful framework for understanding, validating, and optimizing memristive devices, offering a general pathway toward the rational design of future analog computing and neuromorphic systems.

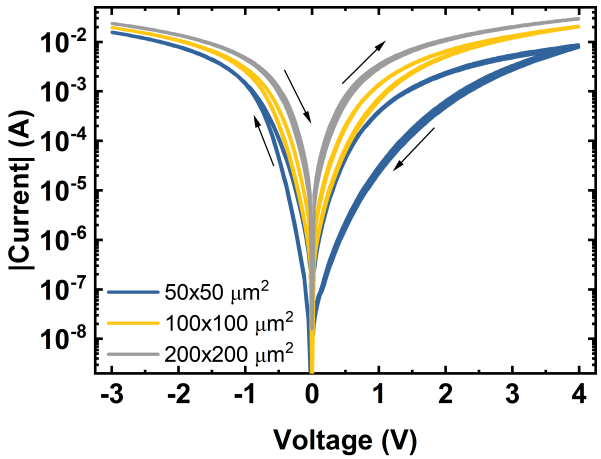


Figure 1. Quasi-static I-V characteristics of Ti/Au TE devices with square side lengths of 50, 100, and 200 µm.

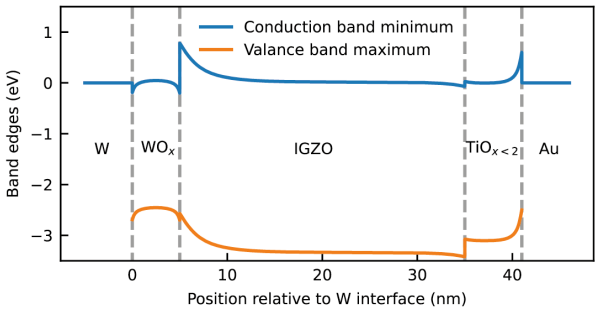


Figure 2. Simulated band diagram for the Ti/Au TE devices.

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Ca-Concentration and Area Dependence of Resistive Switching in $Al/Gd_{1-x}Ca_xMnO_3$ Memristors

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$Al/Gd_{1-x}Ca_xMnO_3$ memristors exhibit resistive switching governed by the active metal/oxide interface, where the motion of oxygen vacancies and modulation of the interfacial oxide layer affect the effective transport barrier. However, the influence of GCMO composition on the scaling behavior and robustness of the resistive states remains insufficiently clarified. In this work, we investigate how the Ca concentration of $Gd_{1-x}Ca_xMnO_3$ and the physical device area affect the electrical characteristics and resistive switching behavior of Al/GCMO memristors.

GCMO thin films with Ca concentrations in the range $0.70 \leq x \leq 0.95$ were deposited on $SrTiO_3$ substrates by PLD. Devices with lateral dimensions from 25×25 μm^2 to 300×300 μm^2 were fabricated using optical lithography, wet chemical etching, and electron-beam evaporation of metal electrodes. The crystallographic properties of the films were characterized by XRD, while film thickness and surface morphology were evaluated by AFM. The electrical and resistive switching properties were measured using Keithley SMUs and an ArC ONE platform.

The results show that the Ca concentration strongly affects both the absolute resistance level and the stability of the resistive states. The most favorable resistive switching behavior was observed for $0.80 \leq x \leq 0.90$, while the most robust high- and low-resistance states for device operation were obtained at $x = 0.90$. For all studied compositions except $x = 0.70$, the device resistance scaled approximately with the inverse of the device area, indicating that the switching is dominated by an interface-type mechanism involving a substantial fraction of the active Al/GCMO contact area. In contrast, the $x = 0.70$ devices showed anomalous area scaling, suggesting a deviation from uniform interface-controlled switching.

These results demonstrate that Ca concentration is a key parameter for tuning both the conductivity and switching reliability of GCMO-based memristors. The observed area scaling supports an interface-mediated resistive switching mechanism for the higher-Ca compositions and provides practical design guidance for scalable Al/GCMO memristive devices.

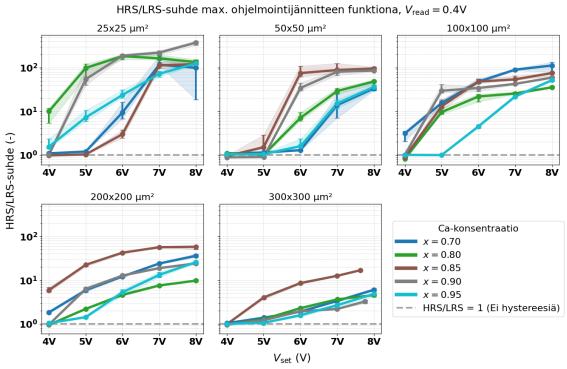


Figure 1. Median HRS/LRS ratios at 0.4 V as a function of SET voltage for different Ca concentrations and device areas. Error bars indicate the interquartile range over ten sweeps.

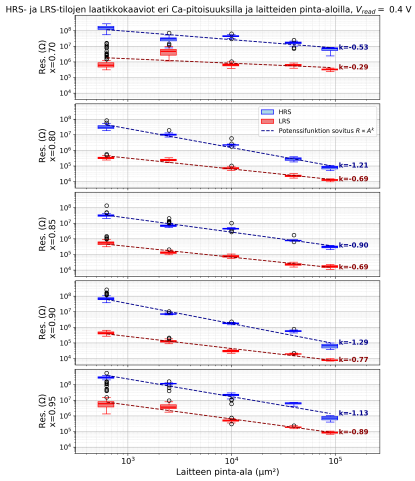


Figure 2. Area scaling of HRS and LRS for different Ca concentrations. Dashed lines are log–log linear fits, with slopes indicating the degree of area-dependent switching.

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Copper(II) halide-acridine complexess new materials for reservoir computing?

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The demand for advanced data processing systems is continuously increasing in the modern world. This trend has stimulated research into novel computing platforms and architectures. One of the promising computational paradigms is reservoir computing, which exploits the nonlinear dynamics of physical systems for efficient information processing. Among the most extensively explored materials in neuromorphic computing are perovskites. However, perovskites often suffer from limited stability [1]. In contrast, metal-organic coordination compounds can offer high stability and broad possibilities for tuning their properties through ligand selection [2].

We present two copper(II)-based complexes for neuromorphic computing. The first material is a copper(II) complex containing four chloride ions and two protonated acridine molecules, $(AKR\text{-}H)_2[CuCl_4]$, while the second contains four bromide ions and two protonated acridine molecules, $(AKR\text{-}H)_2[CuBr_4]$. The structures of these materials were studied using UV-Vis spectroscopy, Fourier-transform infrared spectroscopy, X-ray diffraction, and X-ray absorption spectroscopy. The materials were used to fabricate devices with a metal-semiconductor-metal structure. The complexes show significant structural and spectroscopic differences. Both materials are stable, and their current-voltage characteristics exhibit pinched hysteresis loops. Differences in memristive behavior suggest different switching mechanisms in the two devices. The materials also exhibit higher harmonic generation under large-amplitude sinusoidal voltammetry (LASV), which is promising for applications in reservoir computing.

Reaserch project partly supported by program „Excellence initiative – research university'' for the AGH University of Krakow.

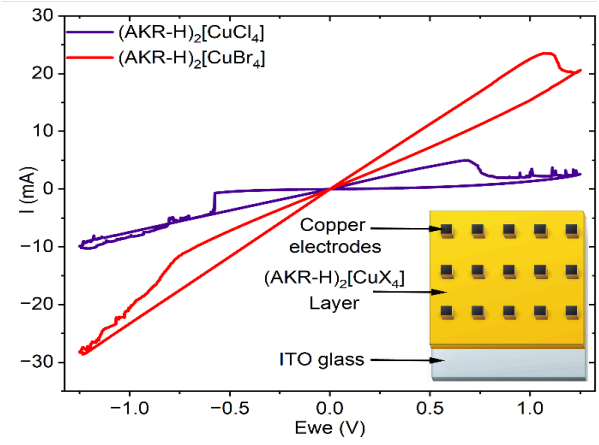


Figure 1. Current-voltage characteristics of both complexess and shceme of the devices.

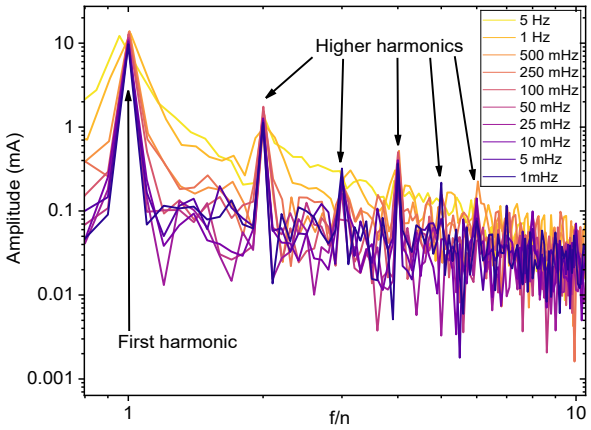


Figure 2. Fourrier transformation of LASV measurements for (AKR-H)2[CuCl4].

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Correlating Resistive Switching with Bias-Induced Chemical Redistribution in Prussian Blue Memristive Devices

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Prussian Blue (PB) is a mixed-valence iron cyanide coordination compound with an open framework structure [1]. Electrodeposited PB thin films have been shown to exhibit reproducible bipolar resistive switching, highlighting their potential for memristive devices [2]. However, the microscopic processes responsible for the resistance modulation remain insufficiently understood. In this work, electrical characterization is combined with analytical transmission electron microscopy (TEM) to investigate bias-induced chemical changes in PB and their possible relation to the resistive switching mechanism.

Ex-situ electrical measurements on approximately 600 nm thick PB films using patterned Au microelectrodes reveal reproducible hysteretic resistive switching over consecutive voltage cycles (Fig. 1).

To investigate electrically induced changes on the nanoscale, electrical biasing experiments were additionally performed inside the TEM istrument using an approximately 2 µm thick PB specimen. Complete bipolar switching could not be achieved in this geometry because the larger film thickness required comparatively high applied voltages, while thermal loading and degradation of the top Au contact limited the accessible bias range. Nevertheless, the electrically stressed specimen was subsequently analyzed by scanning transmission electron microscopy with energy-dispersive X-ray spectroscopy (STEM–EDS). Comparison of pristine and post-bias specimens reveals distinct spatial variations in the elemental distributions, including changes in the potassium and oxygen distribution (Fig. 2), suggesting field-induced chemical redistribution within the PB layer.

In complementary ex-situ experiments, a pronounced local color change was observed near the electrical contact after biasing, consistent with a local change in the PB/Prussian White (PW) redox state. Based on these observations, we propose that the applied electric field promotes redistribution of mobile potassium species, thereby modifying local charge compensation and the Fe2+/Fe3+ balance. The resulting coupled ionic and redox processes may promote local transformations between PB and PW states and contribute to the observed resistance modulation.

The combined electrical and microscopy results are consistent with a switching scenario involving field-induced chemical redistribution and redox changes in Prussian Blue and motivate further in-situ investigations of the microscopic switching mechanism.

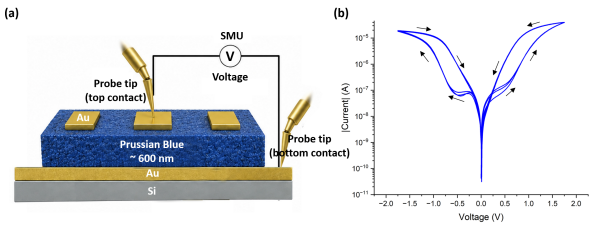


Figure 1. Ex-situ electrical characterization of Prussian Blue thin films. (a) Schematic of the electrical measurement configuration for an approximately 600 nm thick PB film using patterned Au top microelectrodes and an Au bottom electrode. (b) I-V characteristics over consecutive voltage cycles, demonstrating reproducible hysteretic resistive switching.

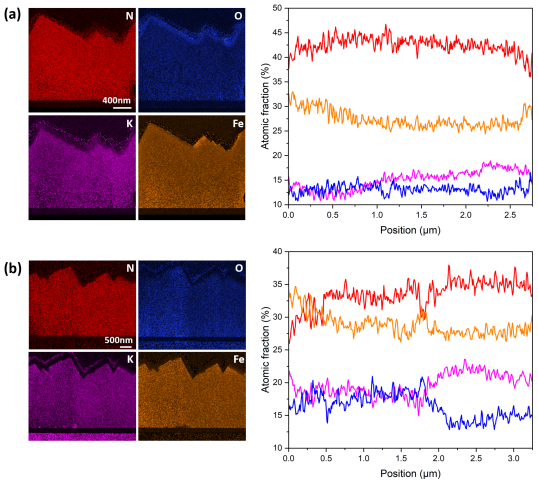


Figure 2. STEM-EDS analysis of Prussian Blue before and after electrical biasing. Elemental maps and corresponding line profiles of N, O, K, and Fe for (a) the pristine and (b) post-bias states. The post-bias specimen exhibits spatial variations in the elemental distributions, especially K and O, consistent with bias-induced chemical redistribution.

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Cu_2O Nanowire Memristors Fabricated in Ion Track-Etched Templates

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We present the fabrication and characterization of Cu_2O nanowire array memristors produced using a template-assisted electrodeposition approach. The nanowire structures are synthesized within ion track-etched polymer templates, which are fabricated by swift heavy-ion irradiation followed by chemical etching. This method enables the realization of highly ordered nanowire arrays with controllable dimensions and high aspect ratios.

The memristive nanowire devices are fabricated through a sequential electrodeposition process consisting of Cu, Cu_2O, and Cu segments deposited within individual template pores, forming metal–oxide–metal nanowire heterostructures. Following template removal, the morphology and structural integrity of the nanowire arrays are investigated by scanning electron microscopy.

Initial electrical characterization is performed by cyclic voltammetry measurements. The obtained current–voltage characteristics exhibit hysteretic behavior consistent with the response expected from memristive systems, indicating the potential of the Cu_2O nanowire heterostructures for resistive switching applications. The influence of the nanowire architecture on the electrical response is discussed, and possible switching mechanisms within the Cu_2O layer are considered.

These results demonstrate a versatile route for the fabrication of nanowire-based memristive devices and provide a foundation for future investigations of their switching characteristics and potential applications in non-volatile memory and neuromorphic computing.

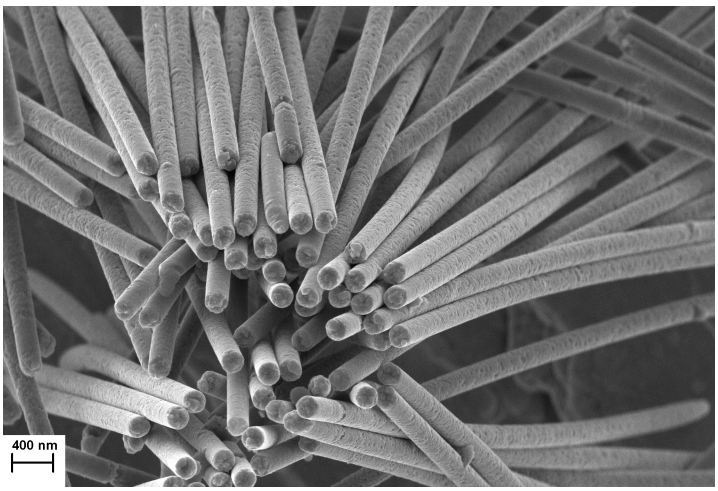


Figure 1. SEM image of Cu/Cu2O/Cu nanowires after template removal.

Design and Characterization of Aminotriazole Iodobismuthate Memristors for Neuromorphic Computing

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The rising energy demands of artificial intelligence have driven increasing interest in computing architectures that move beyond the traditional von Neumann model. Neuromorphic systems offer a promising alternative by combining memory and computation in a way that resembles how biological neural networks work.

A key building block of these systems is the memristive device, which can mimic synaptic behaviour through resistive switching. These devices also allow gradual, analogue-like changes in conductance, making them well suited for implementing learning and memory functions in hardware [1].

Lead-free hybrid organic–inorganic materials are attracting growing interest as active layers for memristive devices in neuromorphic computing. In this work, aminotriazole iodobismuthate complexes are investigated as potential switching media in simple metal–insulator–metal structures [2].

The materials were synthesized as powders using 1,2,4-triazole derivatives with different amine group configurations and subsequently processed into thin films. These layers were integrated into ITO/active layer/metal devices designed to enable interface-driven resistive switching.

Electrical characterization reveals stable bipolar switching behaviour with reproducible ON/OFF states and nonlinear current–voltage characteristics. The switching mechanism is attributed mainly to interfacial effects, likely assisted by ion migration within the hybrid structure. The devices demonstrate good cycle-to-cycle stability and allow controlled modulation of resistance states under repeated biasing.

Neuromorphic functionality was evaluated using potentiation–depression protocols, showing gradual and tunable conductance changes. Additionally, spike-timing-dependent plasticity (STDP) measurements confirm time-dependent weight modulation consistent with synaptic learning rules observed in biological systems. These results indicate that aminotriazole iodobismuthate complexes are promising lead-free active materials for memristive devices and neuromorphic computing applications.

Research project partly supported by program ”Excellence Initiative - Research University” for the AGH University of Krakow

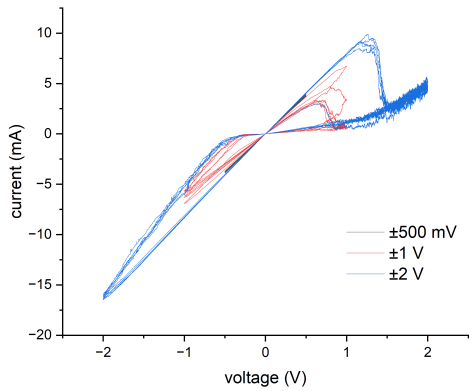


Figure 1. Cyclic voltammetry of a BI_3–4-amino-1,2,4-triazole memristor at different potential scan ranges.

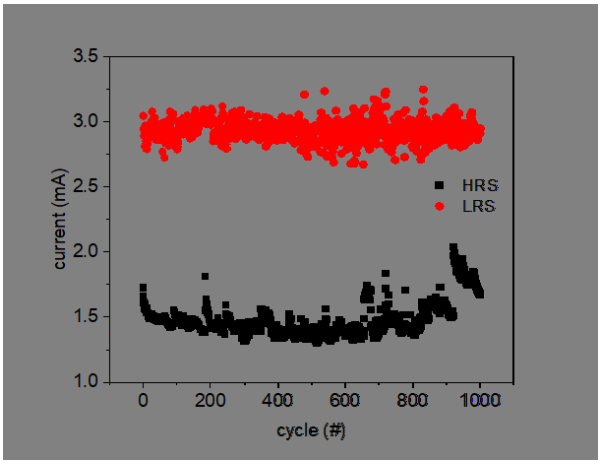


Figure 2. ON/OFF current measurements of a BI_3–3,5-diamino-1,2,4-triazole-based memristor device.

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Engineering Charge Transport in Thiazole-Based Organic and Hybrid Frameworks for Neuromorphic Resistive Switching

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The development of robust, tunable resistive switching layers is a critical milestone in advancing memristive devices for novel computing architectures. By evaluating hybrid copper(I) and silver(I)-cyanothiazole (CuI-CNtz, AgNO3-CNtz) frameworks[1], alongside purely organic thiazolothiazoles (TzTzs)[2] we demonstrate how structural engineering can precisely dictate resistive switching behavior for specific memory and learning applications.

In the hybrid CuI-CNtz complexes, electrical evaluations utilizing scan-rate-independent I-V hysteresis indicate that resistive switching is governed by an interfacial mechanism rather than the standard formation of conductive filaments. The underlying charge transport relies on the dynamic modulation of a Schottky barrier formed at the metal-semiconductor interface, which is driven by the electrostatic repulsion of electrons trapped and detrapped at metal-induced gap states (MIGS). Notably, the type of conductivity is highly dependent on the cyanothiazole isomer.

The completely organic TzTz derivatives display entirely different electrical characteristics. Current-voltage measurements of these materials reveal almost linear dependencies and temperature-independent conductivity, which firmly rules out both Schottky barrier formation and filamentary switching mechanisms. Instead, resistive switching in these highly conjugated organic layers is facilitated by an electron injection-enhanced electron hopping mechanism. Density functional theory (DFT) calculations confirm that the injection of electrons into the solid lattice, creating negatively charged molecular dimers, dramatically increases the electron coupling matrix elements by up to two orders of magnitude compared to neutral dimers. This charging significantly boosts the probability of electron transfer between neighboring molecules, enabling efficient hopping transport.

Finally, the silver based CNtz frameworks present another type of charge transport mechanism. We show that resistive switching in these systems does not arise solely from electronic band structure, it is governed by bias-induced modification of charge injection conditions rather than formation of extended conductive filaments. The electrical response is consistent with a trap-assisted transport mechanism, in which charge carriers localize at coordination-induced defect states, while field-assisted ionic rearrangements within the soft Ag(I) coordination environment modulate conductive pathways. The resulting switching behaviour therefore emerges from a coupled ionic–electronic mechanism, in which the electronic structure governs carrier injection and localization, while ionic dynamics control the formation and retention of conductive states.

In summary, the sources prove that thiazole-based platforms offer a highly adaptable foundation for resistive switching technologies. By selectively modifying either molecular isomerism, organic functional groups, and central metal ions, we can actively influence dominant charge transport pathways. These structurally tunable properties make it possible to meet the demands of next-generation volatile and non-volatile neuromorphic computing systems.

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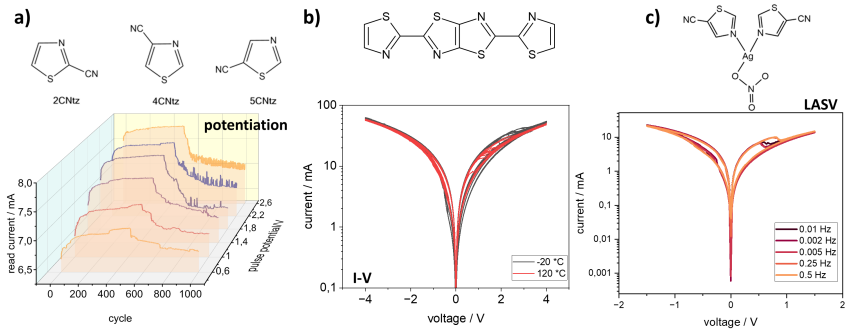


Figure 1. Different types of electrical responses of a) CuI-CNtz, b) TzTz and c) AgNO3-CNtz componds

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Enhanced 2D MoTe2 Analogue Switching Through Laser Processing and ALD-Passivation for Dual-Function Neuromorphic Devices

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Neuro-based computing, enabled by memristors and memtransistors, has drawn significant attention, with Two-dimensional (2D) molybdenum ditelluride ($MoTe_2$) emerging as a promising candidate for its low phase-change energy barrier and tunable electrical behavior. However, realizing the full potential of MoTe2 for neuromorphic applications has been hindered by the lack of a sufficiently large memory window in pristine devices. In this work, we present an effective method to significantly enhance the analogue switching of lateral MoTe2 devices. This method involves two sequential processes: laser treatment followed by atomic layer deposition of Al_2O_3. The synergistic effects of both processes yielded significant performance improvements, with a 70-fold improvement in dynamic range when operating as a memristor and a 20-fold enhancement when functioning as a memtransistor. Consequently, artificial neural network simulations demonstrated 10-fold enhancement in pattern recognition accuracy, while the dual memristor/memtransistor capability enabled the emulation of both homosynaptic and heterosynaptic plasticity.

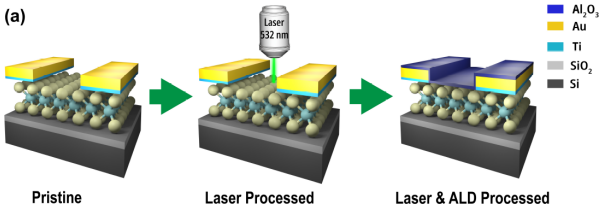


Figure 1. a) Schematic of pristine, laser processed, and laser & ALD processed MoTe2 devices.

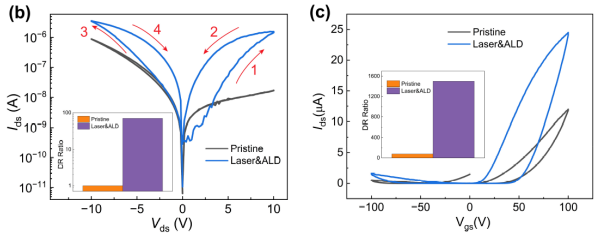


Figure 2. b) Ids-Vds characteristics of the pristine and processed (laser & ALD) MoTe2 memristors. The inset shows dynamic range (DR) ratio for both memristors (DR calculated at Vds = 2V). c) Ids-Vgs characteristics of the pristine and processed (laser & ALD) MoTe2 memtransistors at Vds=1 V. The inset shows DR ratio for both memtransistors (DR calculated at Vgs = 25V). The laser & ALD processed device was optically treated for 10 min with 532 nm laser beam, followed by the ALD deposition of 20 nm Al2O3 at 130 °C [1].

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Enhanced Synapse Performances of Cu:Te/TaOx/IGZO Memristor by Interface Engineering

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Recent advances in AI technology have exposed numerous bottleneck-related issues within traditional von Neumann computing architectures. As an alternative to the architecture, neuromorphic computing architectures are gaining attention due to their low power consumption and large-scale parallel processing capabilities. Among memristors that mimic synapses in biological neural networks, RRAM is particularly suitable for neuromorphic computing due to its advantages of multi-states and linearity in conductance changes. The required synaptic parameters include linearity in conductance changes and dynamic on/off ratio in LTP and LTD curves. Analog SGD minimizes the discrepancy between the desired gradient and the update actually generated by the hardware. In non-linear cases, some weights are over-updated while others are under-updated, ultimately failing to reach the precise target conductance and degrading performance in terms of accuracy and energy consumption. The higher dynamic on/off ratio and linearity are suitable for neuromorphic computing. Previously, numerous studies have been conducted to enhance the on/off ratio and linearity, such as inserting thermal enhancement layers or current limiting layers. However, few cases have been reported that simultaneously achieved both on/off ratio and linearity performance. To address this issue, we adopted IGZO layer. By inserting a bi-layer in IGZO, we could simultaneously control both the Schottky barrier resistance and bulk resistance over a wide range. As a result, we achieved a high dynamic on/off ratio and low non-linearity. The memristor bit accuracy of the optimized device reached a about 7-bits. By successfully integrating the device onto a 16x16 transistor arrays, we obtained a computing bit accuracy of about 6.1 bits and achieved 35 multi-levels. This successfully developed a device suitable for neuromorphic computing.

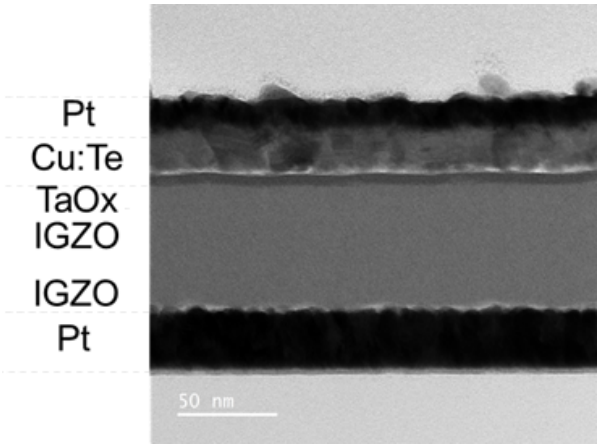


Figure 1. XTEM image of Cu:Te/TaOx/IGZO memristor

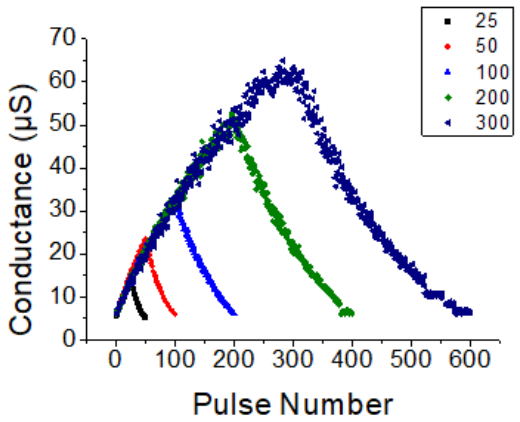


Figure 2. Conductance update curves of Cu:Te/TaOx/IGZO memristor with increasing the number of LTP/LTD pulses

Geometric Confinement of Silver Filament Growth in a Nanostructured Polymer Electrolyte for ECM Memristors

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Electrochemical metallization (ECM) memristors switch through the formation and dissolution of metallic filaments between two electrodes. However, filament morphology is often treated as a stochastic outcome of the switching process rather than as a parameter that can be deliberately engineered. Here, we study Ag filament growth in a coplanar Ag/Pt ECM platform based on a solid poly(ethylene oxide)–silver triflate (PEO–AgOTf) polymer electrolyte.[1] The switching layer is nanostructured with a nonconductive phase that defines PEO-rich ion-conducting pathways and controls the local geometry available for Ag deposition.

We quantitatively analyze how spatial confinement modifies filament growth by extracting morphology metrics, including branching density, lateral spreading, area filling fraction, and bridge probability. Reducing the characteristic spacing of the confining features shifts Ag deposition from sparse, dendritic propagation toward more laterally distributed, space-filling growth. These changes indicate that nanoscale electrolyte geometry can redirect the electrochemical growth front and influence the formation of conductive bridges across the electrode gap.[2] These results provide a design direction for controlling filament formation, which may help reduce variability in future polymer-electrolyte ECM devices.

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Impact of Electrode Materials on the Switching Behaviors of TaOx-based ReRAM Systems: Roles of Schottky and Redox Barriers.

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Redox-based resistive random access memory (ReRAM) has attracted considerable attention owing to its simple metal–insulator–metal (MIM) structure and promising applications in nonvolatile memory and neuromorphic computing. Among various insulating switching materials, tantalum oxide (TaOx) is one of the most widely studied solid electrolytes because it can exhibit both electrochemical metallization (ECM) and valence change mechanism (VCM) switching behaviors depending on the choice of active electrodes [1]. However, the roles of interfacial barriers in governing the underlying switching processes remain unclear.

In this work, two sets of TaOx-based ReRAM systems, namely Cu/TaOx/metal and Ta/TaOx/metal (metal = Pt, Ti, Ta, W, TiN, Au and IrOx), were designed to systematically investigate the effects of electrode materials on ECM and VCM switching behaviors. The Cu-based devices were designed to elucidate the influence of Schottky barriers on ECM switching, while the Ta-based devices were intended to study the impact of redox barriers on VCM switching. Electrical characteristics, including current–voltage (I–V) sweeps, switching kinetics, retention, and endurance, will be comprehensively evaluated and analyzed. In addition, thicker TaOx devices with identical electrode configurations will be fabricated for cyclic voltammetry measurements to characterize interfacial redox reactions.

The results will provide fundamental insights into the interplay between Schottky and redox barriers in TaOx memristive systems and establish electrode-engineering guidelines for designing high-performance ReRAM devices with improved switching speed, reliability, and energy efficiency.

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Influence of Polymer Residue and Top Electrode Deposition Method on MOCVD MoS2 Memristors

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Memristors based on 2D materials such as MoS2 offer promising potential for future memory and neuromorphic applications [1-3]. However, integrating 2D materials into device fabrication remains challenging. Typically, the 2D material is etched before the top electrode (TE) deposition, leaving polymer residues difficult to remove [1,4]. This may interfere with the resistive switching (RS) behavior, either by blocking metal diffusion or by introducing parasitic RS effects [2]. Moreover, metal deposition can damage the fragile 2D layers [3]. To address these challenges, we compare MoS2 memristors fabricated with aluminum (Al) TEs deposited either before or after MoS2 etching, using both evaporation and sputtering.

Here we show that polymer residues remaining after MoS2 etching can inhibit resistive switching in memristor devices. In samples where MoS2 was etched before TE deposition, a thick polymer layer remained on the surface (Fig. 1a), and none of the 40 tested devices exhibited RS behavior. This suggests the residue layer acts as an insulating barrier, preventing the formation or rupture of conductive filaments. In contrast, devices where TE was deposited prior to MoS2 etching showed a high yield of switching behavior. Fig. 1b presents 138 I-V curves from a representative device in which the Al TE was evaporated before MoS2 etching. Switching voltage and resistance state distributions from 40 sputtered and 40 evaporated Al devices (344 and 1560 cycles, respectively) are shown in Fig. 1c and d, indicating similar variability independent of the deposition method. The fabrication technique critically impacts the yield of 2D memristors, while their switching behavior remains consistent.

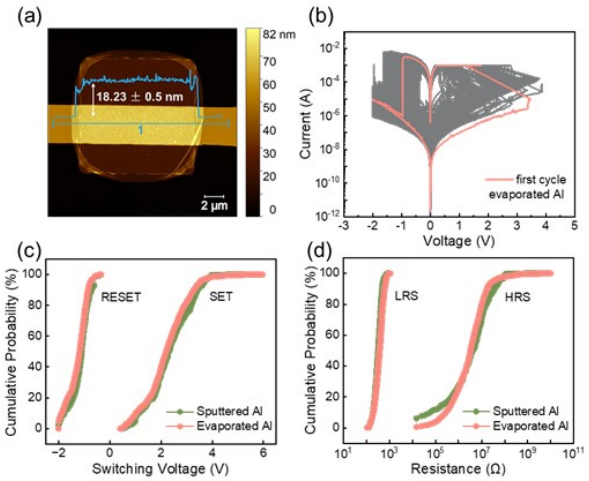


Figure 1. (a) AFM scan of the active area of MoS2 etched before the TE deposition. The BE and the polymer pad are visible. The thickness of polymer residue and MoS2 is 18.23 ± 0.5nm. (b) 138 bipolar I-V curves of an evaporated Al device. (c) SET and RESET voltage distribution comparison between sputtered and evaporated Al samples. (d) HRS and LRS distribution.

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Interface engineering in HZO-Based Memristive Devices for Neuromorphic Computing Applications

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Memristive devices based on oxide materials are promising candidates for next-generation non-volatile memory and neuromorphic computing due to their low power consumption and analog switching capabilities. In this work, we investigate La0.7Sr0.3CoO3 (LSCO) and Hf0.5Zr0.5O2 (HZO)-based potential memristive structures, focusing on the role of the interface in controlling resistive switching behavior. The influence of oxygen vacancy dynamics and ferroelectric polarization in HZO on device performance is studied through electrical characterization, including switching behavior, retention, endurance, and conductance modulation. The coupling between LSCO conductivity and HZO ferroelectric properties enables tunable resistance states, demonstrating potential for artificial synaptic devices. These results highlight new heterostructures as promising platforms for energy-efficient memory and neuromorphic applications.

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Intermediate Resistive State in Wafer-Scale MoS2 Memristors through Lateral Silver Filament Growth

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Memristors based on 2D materials have garnered significant attention. Their fast resistive switching (RS) behavior and atomic-level thickness enable low power consumption, making them promising candidates for neuromorphic computing[1,2]. Among these, memristors based on MoS2 have been extensively studied[3-5]. Their RS has been attributed to the formation and rupture of conductive filaments (CFs). However, the underlying mechanism of filament formation remains underexplored, and the inherently stochastic nature of RS leads to high variability and limited reproducibility. In this study[6], we demonstrate wafer-scale memristors based on MOCVD MoS2 (Fig. 1a). We observe stable RS characteristics in an intermediate resistive state (IRS), set and reset voltages within ±1 V. Combined experimental and simulation results further indicate that the IRS arises from the lateral growth of CFs in the van der Waals (vdW) gaps.

We tested a pristine device beginning with a Icc of 100 μA. As shown by the 35 darker I–V curves in Fig. 1b, the device transitioned from the HRS to an IRS at a Vset of approximately 0.35 V, where the current abruptly rose to the Icc limit. The IRS was retained after the voltage returned to 0 V. Upon applying a negative voltage, the device switched back to the HRS at a Vreset of ∼−0.3 V. Note that we define this state as an IRS because our devices can subsequently switch into a true LRS with significantly lower resistance, and the IRS is both electrically and mechanistically distinct from the LRS. We attribute this non-resettable failure to desulfurization of the MoS2 and the development of a critical gap size between the TE and the filament, accompanied by suppressed filament retraction. Eventually, the accumulated remnant filament can no longer be ruptured by the applied reverse bias, leaving the device irreversibly set to the IRS. After stabilization in the IRS, we increased the Icc to 1 mA and observed further switching into the LRS. While the same measurement protocol was used, the RS between the IRS and the LRS was notably more gradual than the abrupt RS during the HRS ↔ IRS transitions, which we attributed to the lateral expansion of the Ag CF.

The schematics in Fig. 2a,b illustrate the electrochemical metallization cell structure with layered MoS2 and the proposed internal filament morphologies for the IRS and LRS states, respectively. We suggest a bulky, fully formed core structure for the IRS, whereas dendritic arms and layered features develop within the vdW gaps of the 2D MoS2 for the LRS, as illustrated in Fig. 2c. These dendrites can form quantum point contacts with the Ag TE and drastically increase the area of the conductive filament, thereby increasing the current and reducing the resistance. Based on our data and interpretation, we

propose that lateral filament growth is particularly pronounced in layered 2D materials such as MoS2, where the vdW gaps act as preferential channels for Ag+ ion migration and filament expansion, giving rise to distinct, abrupt, or gradual RS behavior governed by the intrinsic anisotropic properties of the material.

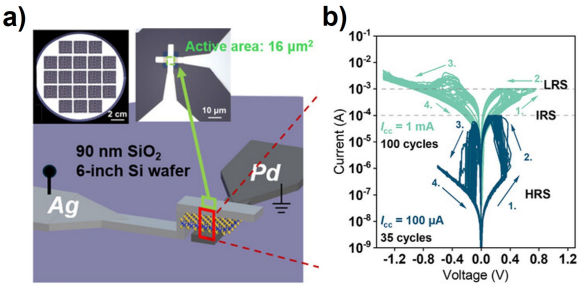


Figure 1. (a) Schematic of a cross-point Ag/MoS2/Pd memristor with an active area of 4 × 4 µm2 on a 6-inch Si wafer with 90 nm SiO2 dielectrics. The inset optical microscopy images show the fabricated 6-inch wafer (left) and a single cross-point device (right). (b) NVS characteristic curves of the device. Under an Icc of 100 µA (dark curves), the device shows 35 NVS curves with an abrupt set process (HRS ↔ IRS), after which switching ceases at this Icc. Upon increasing Icc to 1 mA (light curves), the device exhibited at least 100 stable NVS cycles (IRS ↔ LRS).

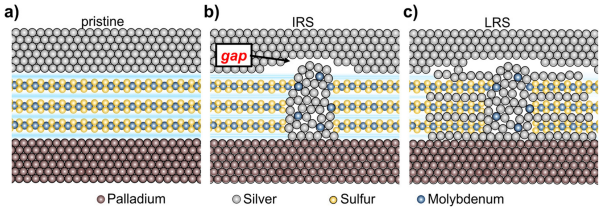


Figure 2. Three different internal states of the reported 2D MoS2 cell: (a) pristine, (b) IRS, and (c) LRS. During IRS switching, the MoS2 lattice is disrupted due to desulfurization, inhibiting further filament dissolution. During IRS ↔ LRS switching, the mechanism changes due to the anisotropic ionic conductivity of the 2D material. Enhanced ionic transport along the lateral vdW gaps promotes the formation of dendrites, resulting in a composite filament consisting of a mixed Ag/Mo bulk material with Ag dendrites extending laterally to further reduce the resistance. For clarity, only three MoS2 layers are shown in the schematic. The gap between the active electrode and the filament is indicated in (b).

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Investigation of Cu2O and STO as oxide layers for memristive devices.

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With communication technology rapidly evolving, driven by increased incentive for higher data speeds and less energy consumption, oxide-based resistive switches, often called memristors, have emerged as promising candidates to aide in pushing communication technology forward. Theorized by Prof. Leon Chua in 1971, memristors are a form of solid state device. Reasons for the hype around them stem from their potential for non-volatile memory, volatile resistive switching, rapid switching capabilities and lower power consumption. This could allow for communication systems that are faster and more energy efficient, while also having the potential to contribute to advances in neuromorphic computing. A result of the ability of volatile switches to emulate the behaviour of neurons and synapses [1,2,3]. Our recent work has focused on Cu2O and SrTiO3 (STO) based devices, with general goals being to characterize their memristive properties. This is to assess their applicability to advanced communication and memory storage (non-volatile switching) and neuromorphic computing (volatile switching). These devices are generally believed to adhere to a valence change switching mechanism due to the device composition, with inert Au electrodes with the oxide layer (Cu2O or STO) sandwiched between, leaving oxygen vacancies as the main migratory material which would act to form the conducting filaments (CFs) for switching [1,4]. Device characterization has been done using atomic force microscopy (AFM) to assess layer thickness and surface roughness, and primarily with I-V measurements to assess memristive properties. In addition to device characterization, the candidate oxide layers have been studied separately using prepared thin films so that the materials themselves could be assessed. X-ray reflection and diffraction (XRR, XRD) have been used to review crystal properties, layer thickness and density. We are currently using x-ray photoelectron spectroscopy (XPS) and argon sputter etching in tandem to perform a depth profile of STO and Cu2O thin films in order to see how material properties (such as Oxygen content) change as upper layers of the films are removed. We will continue with these studies over the next few months in addition to device analysis in an attempt to better understand how the oxide composition changes at different depths within the layer.

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Ion Beam-Induced Defect Engineering of Titanium Oxide-Based RRAM Devices for Emerging Non-Volatile Memory Technologies

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Ion beam irradiation is an effective tool for modifying the structural and electrical properties of materials [1]. This allows controlled introduction of defects in specific areas thus making it an effective tool to improve oxide based electronic devices. Such methodology is of particular importance for the advanced memory technologies such as Resistive Random Access Memory (RRAM), where the configuration and density of defects affect significantly the resistive switching characteristics of the device [2].

In this study, we examine the effect of low-energy krypton (Kr) ion irradiation on titanium oxide (TiOx) thin films used in RRAM devices. The TiOx films were deposited at room temperature using RF magnetron sputtering. Irradiation was performed with 100 keV Kr ions at different fluences (3×10^{15}, 1×10^{16}, and 3×10^{16} ions/cm^2) using an ECR-based low-energy accelerator at IUAC, New Delhi. Electrical measurements were carried out on Au/TiOx/ITO device structures. The results indicate that the as-fabricated TiOx devices did not show resistive switching behavior; however, after Kr ion irradiation, the devices exhibited a significant improvement in performance, achieving a resistance ratio of approximately 10^2.

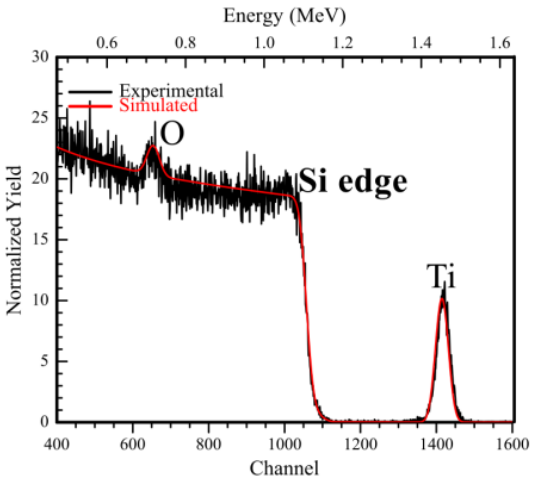


Figure 1. Experimental and simulated RBS spectra of pristine film

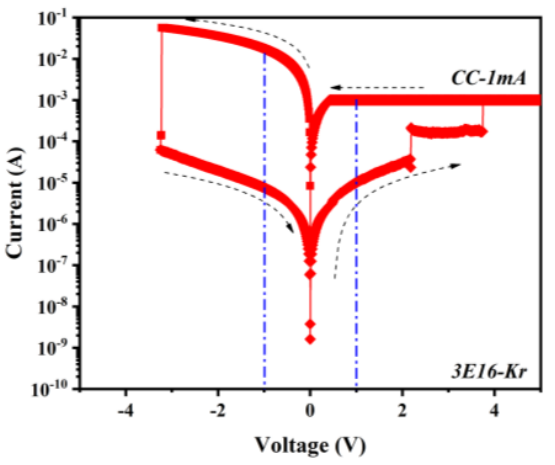


Figure 2. I-V characteristics of 3×1016 Kr ion irradiated device

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Material-generated ionic fluctuations in angstrom-scale two-dimensional nanochannels

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Fluctuations are intrinsic to physical systems and can provide direct insight into the microscopic dynamics of matter under confinement. Here we investigate material-generated ionic fluctuations in angstrom-scale two-dimensional nanochannels, where ions are transported through atomically confined liquid pathways formed between layered crystals. The device consists of a two-dimensional channel defined by an ultrathin spacer between top and bottom crystals, with ionic access provided through microfabricated reservoirs and driven by an applied electric bias.

We find that monolayer-confined ionic transport produces pronounced, controllable current fluctuations that depend sensitively on voltage and device history. At low bias, the ionic current remains in a relatively stable state with weak fluctuations. At intermediate bias, the channel exhibits intermittent switching and burst-like current events, while at higher bias the dynamics evolve into more disordered hopping between fluctuating current states. These behaviours indicate that ionic motion under extreme confinement is governed not only by the instantaneous electric field, but also by slow internal state variables associated with the confined channel environment.

A minimal physical picture based on a multi-stable transport landscape coupled to a slow history-dependent variable captures the observed transition from stable conduction to intermittent bursting and high-bias fluctuating dynamics. These results show that angstrom-scale ionic nanochannels can act as compact physical sources of structured ionic fluctuations, offering a platform for studying non-equilibrium transport, memory effects and fluctuation dynamics in confined ionic systems.

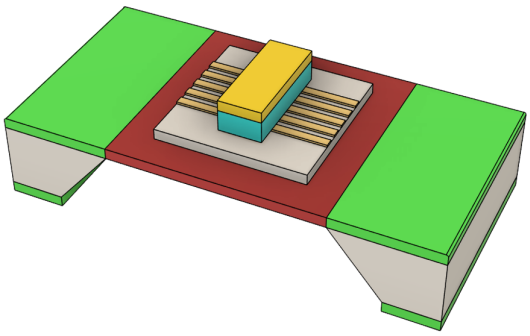


Figure 1. Schematic of the two-dimensional nanochannel device

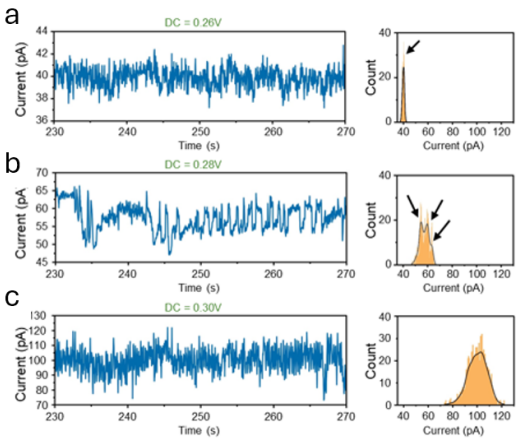


Figure 2. a-c, Ionic current traces and current-amplitude distributions recorded under closely spaced DC biases from 0.26 to 0.30 V.

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Memristive Properties of Dithienopyrrole Polymers in Planar Interdigitated Devices

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Organic memristive materials based on carbazole-functionalized dithienopyrrole polymers are promising for neuromorphic electronics because their electrical properties can be tuned by chemical structure. In this work, dithienopyrrole polymers with functional carbazole side group interconnected via alkyl linker doped with tetrabutylammonium hexafluorophosphate ($TBAPF_6$) wa studied. The main goal was to investigate their switching behaviour under pulsed electrical signals. Thin polymer films were deposited on planar substrates with interdigitated electrodes to prepare lateral two-terminal devices. $TBAPF_6$ was added to the polymer matrix in concentrations up to 10 wt.% to improve charge transport and ion mobility. The electrical behaviour of the devices was evaluated by pulse measurements. Repeated voltage pulses caused gradual and reversible changes in conductance, which confirmed memristive behaviour with several accessible resistance states. In addition, the devices were subjected to 200,000 switching pulses without any significant degradation of their electrical characteristics, demonstrating good operational stability and endurance.The influence of polymer structure and electrolyte concentration on the switching dynamics was analysed and compared with the conductance changes. The results show that both the molecular structure and the amount of electrolyte strongly affect the resistive switching properties and can be used to optimize polymer-based memristive devices for neuromorphic applications.

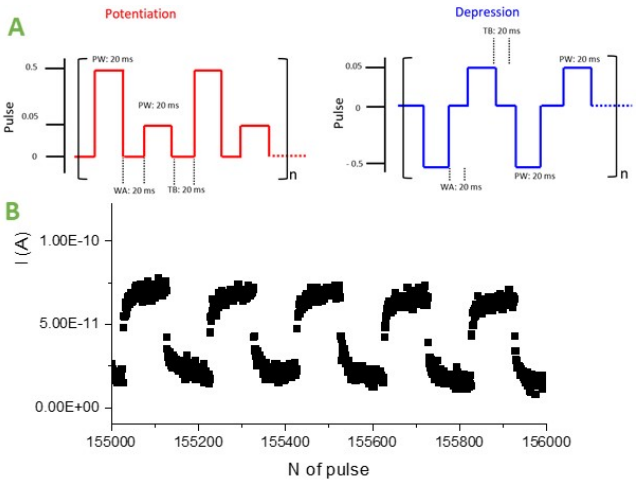


Figure 1. (A) Schematic of the applied voltage pulse train, (B) Current response as a function of pulse number during the application of the pulse sequence shown in (A)

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Mercapto-methylimidazole Molecular Memristors for High-Performance Resistive Switching and Artificial Synaptic Emulation.

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Organic molecule-based memristive devices are promising candidate for next-generation data storage devices for their scalability and low cost. This work discusses resistive memory device based on small organic molecule 2-Mercapto-1-methylimidazole (MMI) and the polymer poly 4-vinylpyridine (PVP), which exhibits stable resistive switching with high on-off ratio (5480), retention over 36K sec and endurance over 700 cycles. In addition to memory behavior, the MMI organic molecule-based memristor exhibits synaptic functions crucial for neuromorphic computing. The device shows analog modulation of conductance in accordance with voltage pulse protocols, which mimicking essential biological learning mechanisms, including potentiation, depression, short-term plasticity (STP), long-term plasticity (LTP), and paired-pulse facilitation (PPF). The device also demonstrates associative learning via Pavlovian conditioning, demonstrating its potential as a hardware-implemented artificial synapse in emerging brain-inspired systems. The carrier transport in these devices follows multiple conduction mechanisms including direct tunneling, trap-free and trap-assisted space-charge limited conduction (SCLC), and Ohmic conduction. The switching is attributed to metallic filament formation from the top electrode which is further supported by impedance measurements. This study highlights the potential of molecular memristors for next-generation memory and neuromorphic computing.

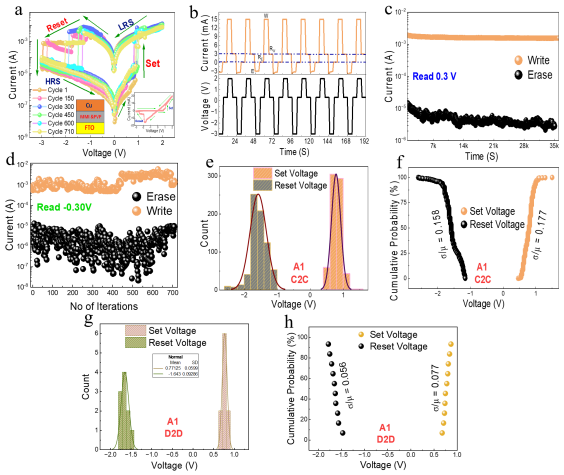


Figure 1. (a) I-V characteristics of Device A1 on a semi-logarithmic scale. (b) The ERWR cycle is used to examine the device's RAM properties. (c) The device's ability to retain data for over 35k seconds demonstrates an excellent retention efficiency. (d) The device's endurance with two distinct resistance states for over 700 cycles. To get a sense of the device's quality, (e) the statistical distribution based on 700 iterative cycles (C2C) with corresponding set and reset voltage is displayed. (f) Cumulative probability based on 700 iterative cycles (C2C) for both set and reset voltages. (g) The device-to-device (D2D) statistical distribution based on 10 A1 devices with corresponding set and reset voltages is displayed. (h) The device-to-device (D2D) Cumulative probability based on 10 A1 devices for both set and reset voltages.

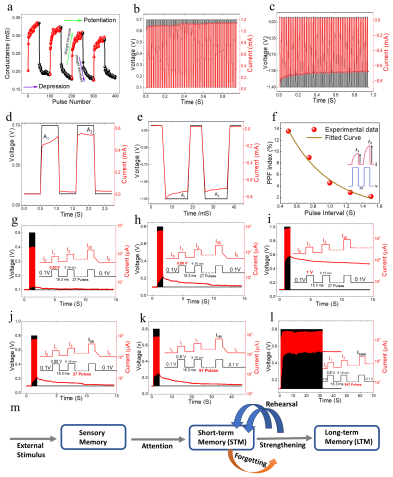


Figure 2. Synaptic behavior in (FTO/MMI&PVP/Cu) device. Fifty (50) positive and fifty (50) negative pulses (Pulse width, 10.5 ms) were applied across four consecutive cycles (400 pulses) to show that potentiation and depression are both consistent and repeatable. (a) Conductance is measured at 0.1 V. (b) Gradual increase in current during Potentiation, (c) Gradual decrease in current during depression. d) PPF at a 0.5 second inter-pulse interval, showing STP. e) Paired-pulse depression (PPD). (f) Decrease in PPF index with an increase in pulse interval from 0.5s to 1.5s. As the pulse amplitude goes from 0.50 V to 1V in device A1, Synaptic plasticity changes from STP to LTP, as shown in figures from (g-i) and Spike-number-dependent plasticity shows that synaptic weight changes from STP to LTP when the number of pulses goes from 30 to 1000, as seen in Figure (j-l) and Synaptic memory model representation for STM to LTM conversion.

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Metastable Defect Engineering for Resistive Switching in $Mo/CdIn_2S_4/Al_2O_3/Pt$ Memristors

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We have recently demonstrated a proof-of-concept memristive device based on a new switching mechanism governed by the reversible charging and discharging of metastable defects in $CdIn_2S_4$ [1]. In contrast to conventional filamentary memristors, the internal state is determined by defect occupation, which modulates the free-carrier concentration and interface barriers without conductive-filament formation or rupture. This mechanism offers potential advantages, including forming-free operation, improved reproducibility, reduced cycle-to-cycle and device-to-device variability, analog conductance control, engineerable relaxation times, and electrical or optical programming. The feasibility of this concept was demonstrated by Zdziebłowski et al. in $Mo/CdIn_2S_4/ZnO–Al$ structures, where metastable-defect charging produced interface-barrier-modulated hysteresis and neuromorphic functionality [1].

As a next step, we introduced a thin Al_2O_3 insulating layer to limit the current and provide additional control over carrier injection and the interfacial potential barrier. The resulting asymmetric $Mo/CdIn_2S_4/Al_2O_3/Pt$ structures were investigated by current–voltage measurements and impedance spectroscopy under different DC-bias conditions. Pronounced asymmetric hysteresis was observed and attributed to bias-driven changes in metastable-defect occupation, carrier redistribution, and modulation of the depletion and tunneling barriers at the two nonequivalent interfaces.

The impedance spectra reveal a continuous transition between capacitive, resistive, inductive, and negative-resistance regimes. Near zero bias, the response is dominated by the series combination of the $CdIn_2S_4$ depletion capacitance and the Al_2O_3 capacitance. With increasing bias, a resistive transport contribution develops together with a low-frequency inductive response. Most importantly, the effective resistance associated with the dynamic transport branch decreases, approaches zero, and becomes negative within selected bias and frequency ranges. The corresponding Nyquist spectra approach an almost vertical line and subsequently cross into the negative-real-impedance region.

Within Bisquert's et al. framework [2,3], this behavior is described by a capacitive branch, a direct transport resistance, and a delayed resistance–inductance branch representing the internal state dynamics of the memristor. The chemical inductance arises because metastable-defect occupation and the associated carrier and barrier redistribution cannot instantaneously follow the AC perturbation. The negative resistance indicates that the defect-mediated feedback becomes locally destabilizing: a small voltage perturbation produces a delayed change in defect occupation that reinforces, rather than suppresses, the current response. This is an active small-signal effect sustained by the applied DC bias and should not be confused with an ordinary passive resistance or with electromagnetic inductance.

In this contribution, we investigate the physical origin of this negative-resistance branch and its relation to metastable-defect charging, interface-barrier modulation, and delayed carrier redistribution. The coexistence of capacitance, chemical inductance, and negative resistance identifies the device as a promising platform for tunable analog memory, artificial synapses, frequency-selective detection, amplification, and, after further optimization, Hopf-bifurcation-driven oscillatory or spiking neuromorphic operation.

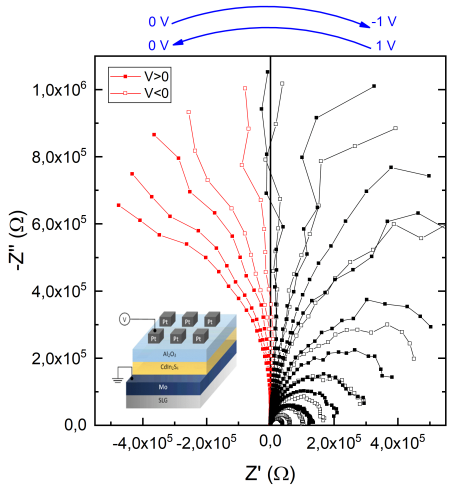


Figure 1. Nyquist impedance spectra of the $Mo/CdIn_2S_4/Al_2O_3/Pt$ device measured under different DC bias voltages together with the corresponding equivalent-circuit. Solid symbols represent positive bias voltages, whereas open symbols correspond to negative bias voltages.

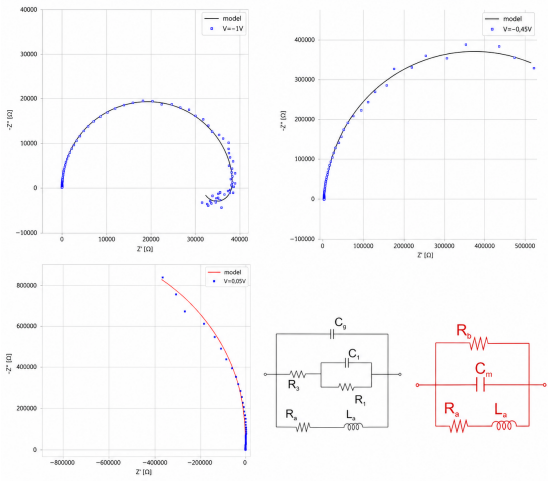


Figure 2. Representative Nyquist plots with fitted equivalent-circuit models (shown in corresponding colors) for selected DC bias voltages. A characteristic low-frequency inductive response is observed at −1 V.

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Modifing the memristive behavior in the RGO-polymer composite films by polyelectrolite exchange

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Excellent endurance, fast switching speed, and high stability are indisputable assets of inorganic memristors. For this reason, technologies based on oxides, chalcogenides, and peroxides are constantly being developed to find the most efficient resistive switching devices. However, their organic counterparts, despite their limited lifespan, are widely used in applications requiring flexibility and biocompatibility, such as wearable sensors and electronic skin. The formation of inorganic-organic composite films allows for the combination of the advantages of both groups of memristive systems, in which the applied polyelectrolytes ensure a homogeneous distribution of the highly conductive inorganic phase. [1]

Accordingly, we have optimized four multilayered systems based on reduced graphene oxide (RGO) and poly(allylamine hydrochloride) (PAH), poly(diallyldimethylammonium chloride) (PDADMAC), poly(ethyleneimine) (PEI), or cationic chitosan. All of the aforementioned systems were obtained using the layer-by-layer (LbL) method via repetitive immersion of ITO glass in polyelectrolyte, water, and RGO suspensions. Through this approach, we obtained well-organized composite films with varying dispersion levels of the nanoadditive.

The distribution of RGO in each multilayer system was examined using AFM and SEM. The deposition process was carefully monitored by QCM-D, which revealed reproducible mass growth after sequential immersions; this growth varied among the applied polyelectrolytes and corresponded to the amount of RGO incorporated into the system. Furthermore, UV-Vis characteristics showed a linear increase in thickness with an increasing number of layers, proving the high reproducibility of the LbL procedure.

The aforementioned dissimilarities in the microstructure of the devices directly affect the memristive behavior of the prestressed system. Cyclic voltammetry demonstrated differences in conductivity, and the size of the memory window depended on the polyelectrolyte used. Additionally, potential depression measurements showed that for all systems, regardless of the applied polymer, the switching potential equals -1.4 V.

Using the additional retention measurements, pattern recognition simulations using MNIST data were performed. Depending on the number of epochs and the complexity of the neural network, the different composite films revealed significant changes in pattern recognition effectiveness. This provides evidence for the high tunability of RGO-polymer memristors based on the specific polyelectrolyte used.

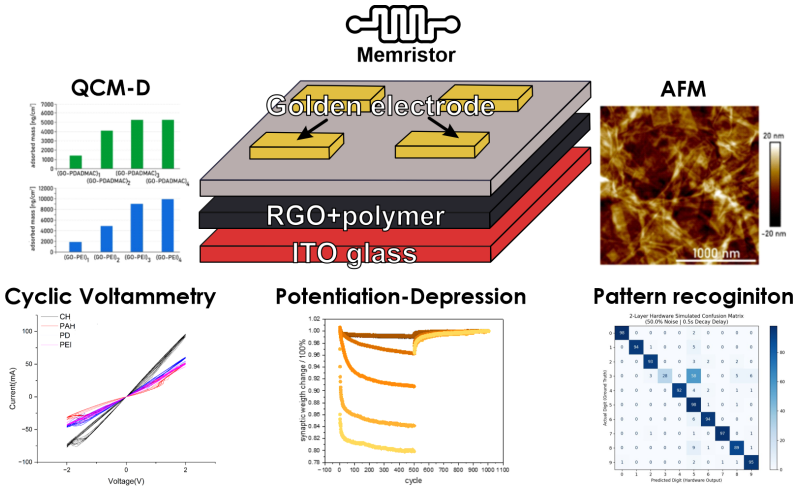


Figure 1. Schematic illustration of the RGO-polymer network memristor alongside representative results

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Multiscale Functional Analysis of Neuromorphic Nanoparticle Networks via In Situ Electron Microscopy Revealing Network Structure-Function Relationship

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Self-organized nanoparticle networks (NPNs) close to their percolation threshold are promising for bio-inspired information processing. These NPNs show non-linear responses, with avalanche criticality similar to those observed in the human brain [1] which is expected to be beneficial for complex task solving. A novel multiscale approach with in situ electron microscopy using electron beam induced current (EBIC) methods, revealed spatially and temporally distributed memristive switching events [2]. These AgAu NPNs are fabricated via magnetron-based NP deposition which was stopped near the electrical percolation threshold by monitoring the current onset. By this, a NPN is formed, where interconnected NP groups are separated by gaps. These are the relevant locations for resistive switching. This study focuses on the characterization of the morphology of NPNs and on potential pathways manipulating their morphology. Here, we complement in situ heating in the scanning transmission electron microscopy (STEM) focusing on the morphology on nanometer-scale with in situ heating in the scanning electron microscope (SEM) focusing on the current path on micrometer-scale.

After 15 min heating at 210 °C, EBIC revealed a fragmentation of the electrically connected NPN area, which was accompanied by an increased resistance. After heating at 240 °C, the NPN turned insulating and the electrically connected NPN area shrunk further(Fig. 1). The NPN could be reactivated to a conducting and spiking state by an electrical stimulus of 18 V - without changing the network size.

These macroscopic findings are complemented by a STEM analysis of a second AgAu NPN which indicated a densification and the formation of coalescenced NPs due to heating. To quantify the observed changes and to relate them to the network properties, a morphological and fractal analysis was performed on the voids in the NPN and on the NPN itself (Fig. 2). This revealed a growing void size by deagglomeration of nanoparticles and fractal properties, indicating a reduced degree of percolation and connectivity due to heating. The fractal analysis is capable to bridge the micro- and the macro-scale and provides the first explanation of how the morphology with scale-free spatial correlations map temporal correlations as observed in avalanche criticality.

These findings provide valuable insights into the stability of neuromorphic NPNs and their tunability for applications such as physical reservoir computing.

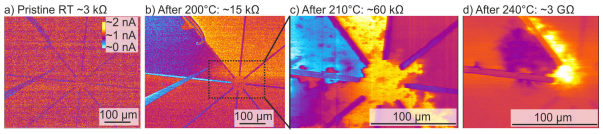


Figure 1. EBIC images after indicated heating steps revealing a fragtmentation of the nanoparticle network and a reduction of the resistance.

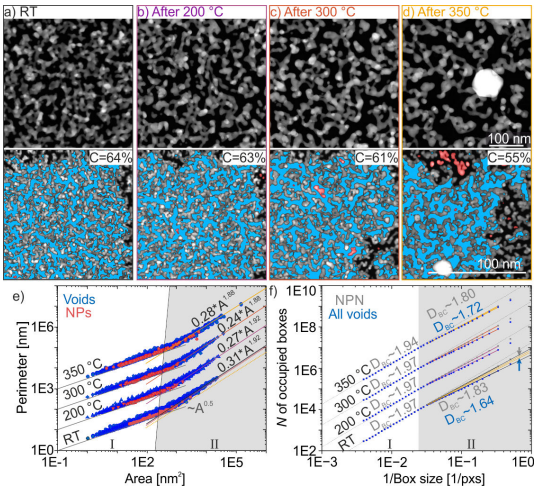


Figure 2. STEM images and fractal analysis of voids and NPN revealling decreasing spatial correlations

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Physics-informed microstructure engineering of HfOx in wafer-scale memristive devices

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Tailored device performance in neuromorphic and nonvolatile memory applications strongly depends on precise microstructure engineering [1]. This can be achieved by linking fabrication parameters to material properties. In widely used material systems such as HfOx, fabricated by industrially adopted reactive magnetron sputtering, microstructural properties, including crystallinity, mechanical strain, and stoichiometry, are governed by deposition parameters such as magnetron power, substrate temperature, and ambient atmosphere. Combined with wafer-scale device integration, this coupling enables a multi-objective optimization framework for achieving reproducible and well-controlled fabrication processes, ultimately leading to uniform device performance across the wafer (Fig. 1).

Conventionally, microstructure engineering involves certain Design-of-Experiments (DoE) methods, e.g., ANOVA or other statistical methods that include polynomial fitting of the extensive experimental datasets [3]. Such an approach, however, has two clear disadvantages: requiring substantial resources and, at the same time, being specific to a very particular process and tool, hardly transferable between other systems. Furthermore, most of the known DoE approaches ignore the physical meaning of the fitted parameters, making a fundamental understanding of the origin of the optimization challenging [4].

We present a physically interpretable conceptual model that captures established cause-and-effect relationships between magnetron sputtering parameters — including the argon-to-oxygen flow ratio — and the resulting material properties [2]. In contrast to conventional trial-and-error approaches, the proposed framework identifies optimized material properties within the investigated parameter space without requiring extensive experimental datasets. By incorporating physically motivated dependencies, the model provides both predictive capability and process insight.

Furthermore, we demonstrate a hierarchical multi-objective decision framework for selecting optimal material characteristics for memristive device fabrication, for example, TiN–HfOx–Al single devices. The resulting devices exhibit uniform performance across the wafer, high electroforming success, and reproducible bipolar switching behavior, demonstrating their suitability for large-area integration.

Our approach provides a systematic and efficient route to accelerating thin-film process development while establishing a scalable framework readily adaptable to other magnetron sputtering processes. Moreover, the framework is extendable to a broad range of materials, including, but not limited to, oxides, and to emerging memory-device architectures.

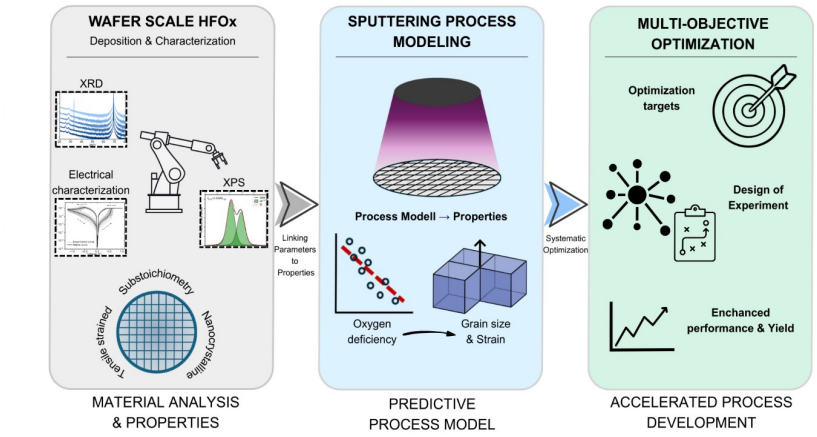


Figure 1. Schematic overview of the optimization strategy—from wafer scale analysis toward multi-objective optimization [2].

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Realisation of Artificial Synapse through Solution-Processed Organic Small Molecule/ZnO Nanoparticle Hybrid Memristor

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Memristors integrate computing and storage within a single device, addressing the inherent constraints of the Von Neumann architecture. They have recently attracted considerable attention due to their capability for high-density storage and neuromorphic computing [1]. Among the various hardware platforms for neuromorphic computing, memristors have attracted significant attention for their ability to emulate synaptic plasticity through tunable conductance states. Organic–inorganic hybrid memristors combine the mechanical flexibility and low-power operation of organic materials with the stability, uniformity, and high switching performance provided by inorganic components [2][3]. In this work, an organic–inorganic hybrid memristor is fabricated using the small molecule 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS Pentacene) blended with ZnO nanoparticles (ZnO NP) as the active layer. The Cu/TIPS Pentacene: ZnO NP/ITO memristor exhibited stable bipolar analog resistive switching with a data retention of 10^5 s and endurance of ∼430 cycles at a low operating voltage of ∼ ±1 V. To evaluate its suitability for artificial synapses, comprehensive neuromorphic measurements are performed. The device demonstrated gradual potentiation and depression under repeated voltage pulse trains, enabling analog weight updates. Synaptic plasticity characteristics, including long-term potentiation/depression (LTP/LTD), spike-rate-dependent plasticity (SRDP), paired-pulse facilitation (PPF), and post-tetanic potentiation (PTP), are clearly observed. Structural characterization of the active film is carried out using transmission electron microscopy (TEM), field-emission scanning electron microscopy (FESEM), and X-ray photoelectron spectroscopy (XPS). Finally, the neuromorphic computing capability of the device is assessed by incorporating the experimentally extracted LTP/LTD characteristics into a convolutional neural network (CNN) for handwritten digit recognition. The organic–inorganic hybrid architecture integrates the high mobility and tunable electrical properties of TIPS Pentacene with the strong charge-trapping capability of ZnO nanoparticles. This synergistic interaction facilitates gradual conductance modulation and improves the linearity of synaptic weight updates.

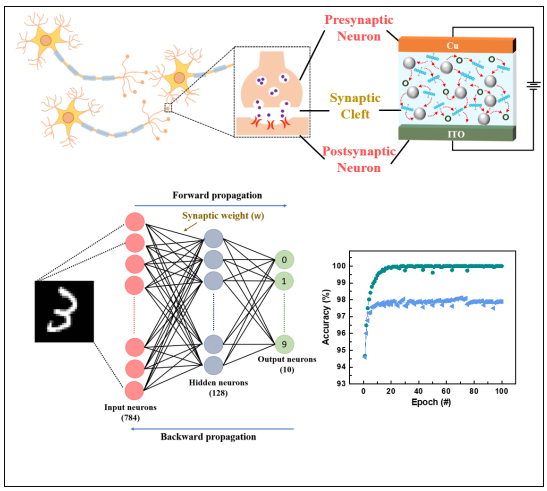


Figure 1. Conceptual representation of the Cu/TIPS-pentacene:ZnO nanoparticle hybrid memristor as an artificial synapse and its application in MNIST handwritten digit recognition

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Size-Dependent Memristive Switching in HfO2 Nanoislands Revealed by Conductive Atomic Force Microscopy.

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To create reliable and precisely controllable high density Resistive Random-Access Memory (RRAM) technology, the nanoscale processes behind the switching mechanism need to be clearly understood. The downscaling of memristive systems means that the scalability of memristive materials in highly confined nanodevices is becoming an ever more important factor. Nanoislands of HfO2, one of the most prominent memristive materials, were previously shown to exhibit a bulk-like bandgap with extra in gap states [1], sparking further interest in the nanoislands electronic behavior, however switching properties of these nanoislands have not yet been reported.

To facilitate this, HfO2 nanoislands are investigated by Conductive tip Atomic Force Microscopy (cAFM), which can simultaneously analyze the topography and electronic properties of surfaces on the nanoscale. By using the cAFM tip as a mobile top-electrode localized resistive switching experiments can be performed in-situ and formed conductive filaments can be visualized. [2,3]

HfO2 nanoislands are grown on the atomically flat Au(111) surface by Pulsed Laser Deposition (PLD) and subsequently analyzed by cAFM in-situ, revealing individual, insulating islands of different sizes. For the first time, local in-situ resistive switching in different islands down to below 10 nm in diameter is demonstrated by using the cAFM tip as a top electrode. The current compliance integrated into the cAFM setup enables monitoring multiple cycles of switching in a single island, showing that the observed resistive switching behavior depends strongly on the applied current compliance, as well as the island size.

A mechanism of two simultaneous processes of oxygen ion movement within the nanoisland is proposed and complemented by simulations of the electronic potential across the tip-island junction for islands of different sizes. At larger currents, the loss of oxygen via the island surface is the dominating feature, continuously decreasing the islands resistance regardless of the applied bias polarity. By moderating the current compliance, oxygen loss is suppressed and the oxygen ion movement within the nanoisland dominates, revealing SET/RESET behavior. Both polarities of switching are observed, with a clear dependence on island size. There is an expected minimum volume required for a conductive filament to form isolated from its surroundings. In larger islands, a filament may dominate the switching behavior, while islands that fall below this minimum are expected to switch as a whole. This is supported by imaging the area before and after tip-induced switching, visualizing changes in the islands conductivity: In larger islands, small conductive spots can be interpreted as a formed filament, for smaller islands the entire structure appears more conductive.

We demonstrate multiple cycles of in-situ resistive switching in a single HfO2 nanoisland by cAFM for the first time. We gain new insights into the scalability of HfO2 as a memristive material and the nanoscale processes underlying the resistive switching behavior, especially the influence of interfaces and spacial confinement regarding the formation of conductive filaments.

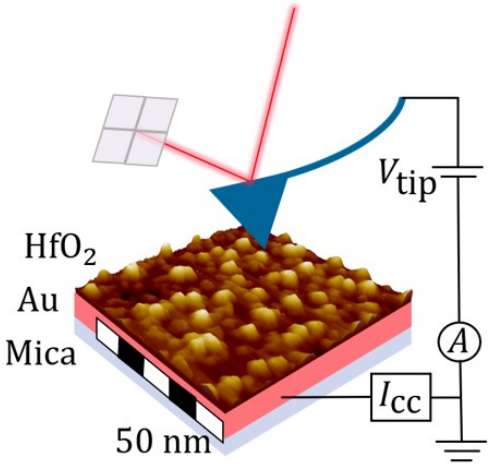


Figure 1. Schematic of cAFM topography and current response measurements of HfO2 nanoislands grown on Au(111)/Mica.

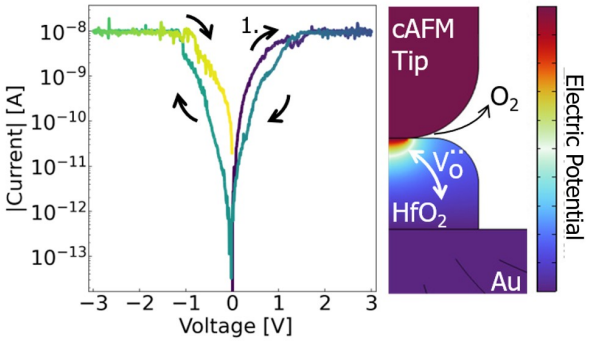


Figure 2. I/V curve showing RESET/SET behavior taken on a single HfO2 island by cAFM and schematic of potential across the tip-island junction under bias with possible oxygen ion movement.

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Structure and Chemistry of Resistive Switching in Yttria-based RRAM

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Yttrium oxide is a wide-bandgap oxide with tunable defect chemistry and high thermal stability, making it a promising candidate for resistive random-access memory (RRAM) applications such as multilevel storage and neuromorphic computing [1-4]. It is highly sensitive to oxygen content; however, its structural distortion, defect chemistry and resistive switching mechanism remain largely unrevealed. Here, we present a combined study of structural, transport and hard X-ray photoelectron spectroscopy (HAXPES) measurements for a detailed exploration of the switching mechanism in yttria based RRAM devices.

Oxygen-engineered yttrium oxide samples were fabricated by reactive molecular beam epitaxy. The structural analysis was conducted by XRD on Y-O/sapphire samples using pole figures and $2\theta/\omega$-scans. The $2\theta/\omega$-scans at different poles show that there is a peak splitting of cubic-(222) and its equivalent planes, which indicates a rhombohedral distortion of the cubic phase. The lattice parameters are calculated as a=10.55 Å and α=89.21°. HAXPES measurements were used to determine the nominal stoichiometry of the samples (Y:O of 1:1, 1:1.2, 2:3) and revealed metallic yttrium content in the most oxygen deficient sample. This sample (nominal composition of YO) shows metallic-like behavior, as its resistivity decreases with decreasing temperature ($d\rho/dT>0$). Optical spectroscopy yields a bandgap of ∼5.7 eV for all stoichiometries.

To investigate the physicochemical processes that govern resistive switching in yttria-based RRAM, devices of Pt/Y2O3/TiN stack composition were fabricated and electrically programmed into pristine, low resistive state (LRS) and high resistive state (HRS) using a Keithley 4200 SCS before the angle resolved HAXPES measurements. In the pristine state, the Y3d core level consists of only one Y-O component at every depth, consistent with the Y2O3 stoichiometry. In contrast, switched devices show a clear metallic component in the Y3d core level. In LRS, the presence of metallic yttrium can be found throughout the yttria layer. On the other hand, in HRS, Y0 is only confined near the top and bottom interfaces, consistent with the ruptured filament.

As the stable valence states of yttrium are 0 and +3, these results suggest that resistive switching in yttria-based RRAM takes place via the formation of an yttrium-rich conduction path, as opposed to the formation of suboxides in other VCM devices or pure metallic filaments in ECM RRAM.

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Synthesis, characterization and Memristive Performance of Tailored Dithieno[3,2-b:2‘,3‘-d]pyrrole Conjugated Polymers

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Memristors, originally proposed by Leon Chua as the fourth fundamental circuit element, combine resistive behavior with non-volatile memory effects [1]. Conjugated polymers represent an attractive class of materials for organic memristive devices due to their tunable molecular architecture and charge transport properties [2,3]. In this work, we investigate a series of carbazole-functionalized dithieno[3,2-b:2’,3’-d]pyrrole (DTP) monomers bearing alkyl spacers of different lengths (C3, C6, C10, and C12) and evaluate the influence of side-chain engineering on the memristive response of the resulting polymers [4].

The monomers were synthesized via palladium-catalyzed Buchwald–Hartwig amination and subsequently electropolymerized on ITO substrates from ACN/0.1 M TBAPF6 electrolyte. Their structures were confirmed by 1H NMR spectroscopy, while polymer formation was verified by FTIR spectroscopy. Additional characterization was performed using XPS, cyclic voltammetry, and UV–Vis spectroscopy.

Systematic variation of the alkyl spacer length enabled investigation of the relationship between molecular flexibility and electrical performance. The shortest spacer (C3) exhibited reduced solubility and limited conformational freedom, resulting in more challenging synthesis and electropolymerization, less homogeneous films, and a weak, unstable memristive response. In contrast, polymers containing longer alkyl spacers formed more uniform layers and demonstrated pronounced, reproducible frequency-dependent I–V hysteresis characteristic of memristive behavior. These findings highlight the critical role of side-chain architecture in governing charge transport and memory effects in DTP-based conjugated polymers and provide guidelines for the molecular design of future organic memristive materials.

Acknowledgments: This work was supported by the Czech Science Foundation (GAČR No. 24 10384S), Ministry of Education, Youth and Sports of the Czech Republic Program INTER-EXCELLENCE II (LUAUS24032) and Internal Grant Agency of TBU in Zlín (IGA/CPS/2026/003).

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Tailoring Resistive Switching Performance in Hafnium Oxide Based Memristive Devices with Crystallinity Engineering

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In memristive crossbar arrays, the application of switching voltages generates Joule heating, which can be leveraged as a functional variable rather than seen as a drawback [1]. Localized heat dissipation enables thermal crosstalk between neighboring devices, enhancing associative learning and potentially lowering the switching voltage threshold [2]. Exploiting this effect deliberately requires maximizing thermal coupling between neighboring memristors, which can be approached through two complementary strategies. The first is architectural, leveraging crossbar array geometry and scaling to control heat distribution pathways. The second is material-based, targeting the microstructure of the switching layer itself. In particular, the crystallinity of the active oxide—including crystallite size and lattice strain—directly governs local thermal conductivity and ionic mobility, and thereby determines both the thermal crosstalk efficiency and the resistive switching performance of individual devices [3]. In this work, the control over both crystallite size and lattice strain, as well as their influence on the resistive switching performance, focusing on parameters such as resistance window, switching voltage, and variability, were systematically investigated.

The fabrication of memristive devices involved a 10 nm thick HfOx layer, comprised of nanocrystallites dispersed within an amorphous matrix, displaying a wide range of orientation distribution. A controllable variation in crystallite size and lattice strain was demonstrated, enabling the investigation of their separate influences on resistive switching parameters. Our findings indicate that crystallinity impacts not only the switching voltages and resistances in different states but also their variability. For instance, resistance variability tends to increase with larger crystallite sizes, while the variability of electroforming voltages decreases. Additionally, the absolute mean values of bipolar SET and RESET voltages show a slight increase as crystallite size increases. At the same time, as tensile strain rises, the resistance window shifts to lower values, the variability of electroforming voltage declines, and the mean SET voltage decreases. Given the uncertainty surrounding the mechanisms underlying these dependencies, we adopt a data-driven surrogate model to learn the cross-scale connections directly from observations.

These findings suggest a transferable modeling framework, indicate that deterministic control of crystallinity may lead to reduced variability, and serve as a basis for exploring how crystallinity-governed thermal conductivity in HfOx shapes Joule heating distribution and thermal crosstalk dynamics across neighboring devices in crossbar arrays.

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The role of thin insulating barriers in amplifying the dynamic range in oxide semiconductor interface based memristors

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Memristive switching in oxide-based metal–semiconductor (MS) junctions is inherently constrained by depletion-controlled transport, limiting the achievable dynamic range of resistance states. Although charge transport across Niobium-doped Strontium Titanate (Nb:STO) interfaces is well established, approaches to overcome this limitation without altering the bulk semiconductor remain underexplored. Here, we combine experimental current–voltage I-V measurements and analytical modeling to demonstrate that inserting an ultrathin aluminum oxide Al2O3 layer between cobalt (Co) and (Nb:STO) (0.1 wt% Nb) fundamentally enhances memristive performance by broadening the resistive switching window. This transition from an MS to a metal–insulator–semiconductor (MIS) architecture redistributes the applied bias, localizing the electric field within the Al2O3 layer due to its dielectric mismatch with Nb:STO. This field concentration reduces the effective tunneling barrier width and promotes field-driven transport across the interface. Analytical calculations quantitatively capture the resulting barrier modulation, showing strong agreement with measured I-V characteristics. Consequently, the MIS device exhibits a significantly increased low-resistance-state current and an expanded dynamic range compared to its MS counterpart. Furthermore, the enhanced dynamic range under forward bias leads to the symmetric DC I-V characteristics in both the Voltage bias regime, enabling to achieve better linearity and symmetric weight updates under the application of appropriate programming pulse schemes. These results establish dielectric interface engineering as a robust, scalable route to overcome depletion-limited switching and provide a general framework for optimizing interface oxide-based neuromorphic hardware.

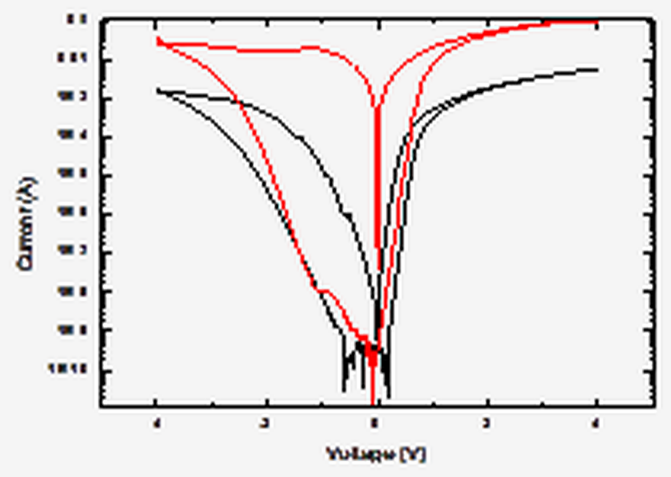


Figure 1. I-V sweep of two different devices MS(black) and MIS (red). MIS device (red) shows a significantly enlarged memristive window, with a much wider current separation between forward and reverse sweeps compared to the MS device. This enhancement arises from the insulating barrier layer, which suppresses the depletion width and amplifies field-driven trap and vacancy dynamics, leading to stronger hysteresis.

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Transition Between Abnormal and Conventional Bipolar Resistive Switching in HfOx-Based Memristors Through Ar/O_2 Ratio Control During RF Sputtering

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Hafnium oxide (HfOx) is one of the most promising high-k dielectrics materials for memristive devices due to its compatibility with complementary metal–oxide–semiconductor (CMOS) technology, scalability, and stable switching characteristics. This makes it a strong candidate for next-generation memory and neuromorphic computing systems that require low-power operation, high storage density, and synaptic functionality[1,2]. Although many studies have investigated the effect of doping, post-deposition treatments, and electrode engineering on device performance, the impact of oxygen incorporation during film deposition remains insufficiently understood, particularly for achieving low-power switching[3,4,5]. In this work, we investigate the impact of the Ar/O_2 gas ratio on the resistive switching behaviour in Au/HfOx/Au structures deposited by reactive sputtering without applying any additional pre- or post-deposition treatments. HfOx thin films were deposited at different oxygen partial pressures using reactive magnetron sputtering, with all other deposition parameters kept constant. The fabricated metal–insulator–metal (MIM) devices consist of a 27 nm thin HfOx layer sandwiched between Au electrodes. Electrical characterisation revealed that varying the oxygen content during deposition resulted in two distinct switching modes forming. Devices fabricated under oxygen-deficient conditions (Ar/O_2 = 15:5 sccm) exhibited abnormal bipolar resistive switching (BRS) behaviour, characterised by butterfly-shaped current–voltage hysteresis loops, as shown in Fig. 1. The abnormal BRS I-V curves exhibited a low resistance state (LRS) to high resistance state (HRS) transition in both voltage polarities and nonzero-crossing with the existence of short circuit current (Isc). This behaviour is attributed to the coexistence of the memristive and the capacitive effect[6,7]. As the applied voltage increases to 5 V, the device switches from HRS to LRS, indicating the SET process. When the bias is reduced from 5 V to 0 V, the device RESETs to HRS. During the negative voltage sweep (0 V to −5 V), the device again gradually SETs to LRS and subsequently RESETs to HRS as the bias returns to 0 V. Analysis of the I–V characteristics confirms that the devices exhibit low-current switching behavior. In contrast, devices deposited at an Ar/O_2 ratio of 15:10 sccm exhibited conventional bipolar memristive switching with reproducible SET and RESET processes, stable resistance states, and comparatively higher switching current (see Fig. 2). The transition from abnormal butterfly-type to standard bipolar resistive switching mechanism is attributed to changes in the defect chemistry of the HfOx layer. These changes are induced entirely by variations in the oxygen partial pressure during deposition. The results suggest that the concentration of oxygen vacancies plays a decisive role in determining the dominant switching mechanism and device performance. These findings demonstrate that precise control of the reactive sputtering atmosphere is an effective approach for tuning the memristor characteristics and achieving low power operation without a need for additional material processing. This offers valuable insight for the development of energy-efficient memory and neuromorphic computing devices.

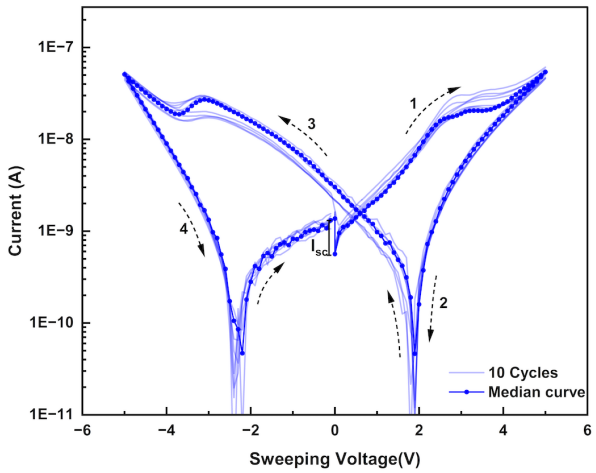


Figure 1. I-V curve of the HfOx memristor exhibiting abnormal (butterfly-like) bipolar resistive switching behaviour fabricated with an Ar/O_2 flow ratio of 15:5 sccm.

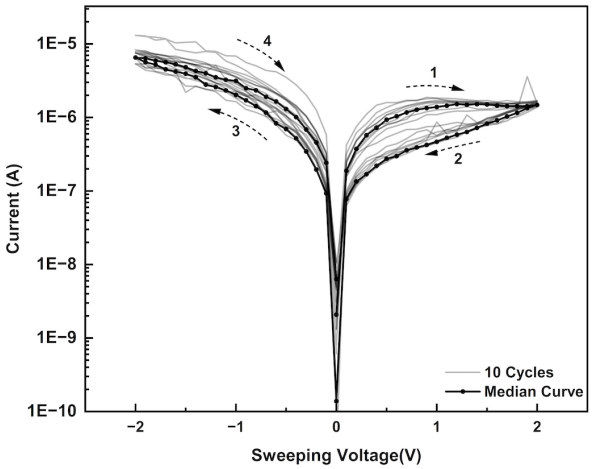


Figure 2. I-V curve of of the HfOx memristor exhibiting conventional bipolar resistive switching behaviour fabricated with an Ar/O_2 flow ratio of 15:10 sccm.

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Tungsten-Doped VO2 Volatile Threshold Memristor for Neuromorphic Computing

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Vanadium dioxide (VO_2) is a promising material for neuromorphic and in-memory computing because its metal-insulator transition (MIT) provides strong nonlinearity, volatile threshold switching, and thermally driven temporal dynamics[1]. In this work, we first demonstrate Pt/VO_2/Pt crossbar devices fabricated from ALD-grown VO_2 as physical reservoirs for Morse-code recognition. The device geometry and SEM image are shown in Fig. 1a. The devices show reproducible threshold switching in DC measurements (Fig. 1b), while Raman spectroscopy confirms the monoclinic M1 VO_2 phase (Fig. 1c). By exploiting the transient switching dynamics of the VO_2 crossbar, Morse-code input sequences are temporally encoded, masked, and projected into a high-dimensional reservoir state space through virtual nodes (Fig. 1d). A simple readout layer then classifies Morse-code words, demonstrating the potential of VO_2 crossbar devices for compact in-memory temporal computing (Fig. 1e)[2].

In parallel, we investigate material-level tuning of VO_2 through tungsten doping. W incorporation is achieved using an ALD super-cycle strategy, in which VO_x growth cycles are periodically combined with $W(CO)_6$ precursor exposure (Fig. 2b)[3]. Raman spectroscopy shows that the doped films retain VO_2-like structural signatures (Fig. 2c), while electrical measurements reveal modified threshold switching characteristics compared with undoped VO_2 (Fig. 2d). Pulsed measurements further show voltage-dependent transient current responses (Fig. 2e), indicating that W doping provides an additional route to tune the switching threshold and temporal dynamics of VO_2 devices. Together, these results connect crossbar device operation with ALD-based material engineering, offering a pathway toward scalable VO_2 memristor with tunable dynamics for neuromorphic computing.

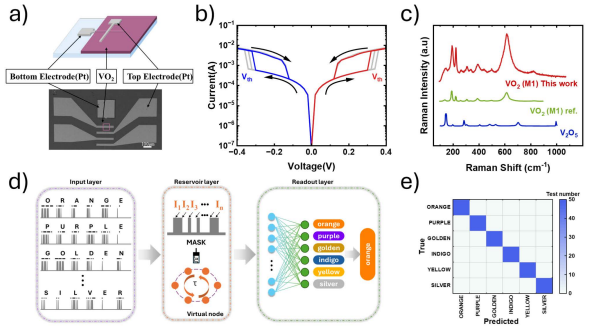


Figure 1. VO_2 crossbar device for Morse-code reservoir computing. (a) Schematic and SEM image of the Pt/VO_2/Pt crossbar device. (b) DC current-voltage characteristics showing volatile threshold switching. (c) Raman spectrum confirming the monoclinic M1 VO_2 phase in the fabricated film. (d) Reservoir-computing workflow for Morse-code word classification using VO_2 dynamics: temporal input patterns are masked and mapped onto virtual reservoir nodes, followed by a trained readout layer. (e) Confusion matrix demonstrating classification of Morse-code words.

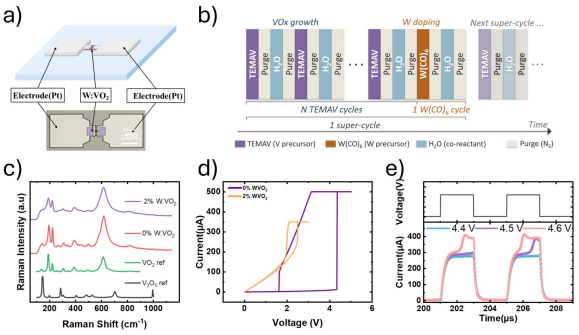


Figure 2. W-doped VO_2 devices enabled by ALD super-cycle engineering. (a) Schematic and optical image of a Pt/W:VO_2/Pt device. (b) ALD process design for W incorporation. (c) Raman spectra of undoped and W-doped VO_2 films. (d) DC current-voltage characteristics comparing undoped and W-doped VO_2 devices, showing modulation of threshold switching behavior. (e) Pulsed electrical response of W-doped VO_2 devices under different voltage amplitudes.

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Tuning Ion Transport and Switching Dynamics in Organic Memristors via Side-Chain Engineering

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As the fourth fundamental passive circuit element, memristors represent a highly viable technology for linking electrical charge to variable resistance for memory retention [1]. Due to their significant potential in neuromorphic engineering, brain-inspired computing, and low-power hardware, current research increasingly focuses on organic electronic materials. These carbon-based systems offer distinct advantages over traditional inorganic semiconductors, including high mechanical flexibility, biocompatibility, and highly tunable electronic properties adjustable through precise macromolecular design and chemical modification [2].

This work investigates a systematic series of novel conjugated polymers based on a dithieno[3,2-b:2′,3′-d]pyrrole (DTP) core featuring varying alkyl side-chain lengths. The monomeric precursors were synthesized utilizing an efficient palladium-catalyzed amination protocol and subsequently electrochemically deposited onto conductive substrates to form stable, uniform thin films. Comprehensive electronic and electrochemical characterization—conducted through cyclic voltammetry, UV-Vis-NIR spectroscopy, and computational modeling—indicates that while the specific length of the peripheral side-chain has a negligible impact on monomeric energy levels, the process of polymerization leads to a significant narrowing of the energy gap along with a pronounced stabilization of the frontier molecular orbitals.

Fabricated two-terminal organic electronic devices exhibit robust, reproducible, and frequency-dependent pinched hysteresis loops, which constitute the definitive fingerprint of memristive systems. The most pronounced memristive response is consistently observed in the low-frequency operating regime [1,3]. This behavior is attributed to the fact that longer timescales associated with low frequencies allow for highly effective ion diffusion within the polymer bulk matrix. Beyond basic resistive switching, the developed devices successfully emulated fundamental biomimetic synaptic functions crucial for artificial neural networks, including long-term potentiation and depression. Under repetitive voltage pulse stimulation, the organic memristors demonstrated a gradual, analog, and reproducible modulation of their electrical conductance states.

A systematic comparative analysis reveals that the exact length of the alkyl substituents significantly influences the resulting current densities, device endurance, and the sharpness of the switching dynamics. These experimental and theoretical findings suggest that while the conjugated polymer backbone dictates the core optoelectronic properties and electronic transport, the flexible side-chains facilitate the supramolecular environment and free volume necessary for efficient ion transport under an applied external electric field [4]. This research establishes side-chain engineering as a viable approach to optimizing organic memristors for upcoming developments in advanced AI hardware and biosensing technology.

Acknowledgments: This work was supported by the Czech Science Foundation (GAČR No. 24-10384S), Ministry of Education, Youth and Sports of the Czech Republic Program INTER-EXCELLENCE II (LUAUS24032) and DKRVO (RP_CPS_2024_28_005) for financial support.

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Posters

Applications

A Brain-Inspired Neuromemristive Synapse for Emulating Homo- and Hetero- Synaptic Plasticity

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Neuromorphic systems inspired by the human brain have attracted significant attention due to their robustness, adaptive learning capability, parallel information processing, multistate memory characteristics, and ultra-low power consumption. However, current bioelectronic technologies still face challenges in accurately reproducing the diverse forms of synaptic plasticity observed in biological systems, particularly the coexistence of homosynaptic and heterosynaptic mechanisms within a single artificial synapse. To address this limitation, this work proposes a neuromemristive synapse capable of emulating a wide range of biologically relevant synaptic behaviors.

The proposed architecture employs a memristor as the core synaptic element owing to its analog switching characteristics, multistate operation, low power consumption, long data retention capability, and compatibility with CMOS technology. In addition to the memristive component, dedicated homosynaptic and heterosynaptic modules are incorporated to regulate synaptic responses under different stimulation conditions. The memristor reproduces synaptic plasticity in response to distinct brainwave-inspired input patterns, while the auxiliary synaptic pathways control the strength and duration of synaptic modifications by governing specific charge and discharge mechanisms. These pathways facilitate the realization of both potentiation and depression processes, enabling the emulation of short-term and long-term memory dynamics.

The proposed synapse was designed and evaluated using SPICE simulations to investigate its functional characteristics and energy efficiency. Simulation results demonstrate that the circuit successfully reproduces several key neurobiological phenomena associated with learning and memory, including short-term facilitation (STF), short-term depression (STD), long-term potentiation (LTP), long-term depression (LTD), memory fading effects (MFE), heterosynaptic facilitation and depression, heterosynaptic homeostasis, input specificity, associativity, and responses to strong stimulation (SST). Furthermore, the synapse exhibits low power consumption while supporting both volatile and non-volatile operating modes.

By integrating multiple forms of synaptic plasticity within a single hardware framework using commercially available components, the proposed neuromemristive synapse provides a biologically plausible and CMOS-compatible solution for next-generation neuromorphic systems. The presented approach has the potential to advance the development of energy-efficient spiking neural networks, large-scale neuromorphic architectures, and computational models for investigating brain-inspired learning and memory processes.

A connection-centric paradigm for biologically detailed neuron simulation using memristive computing-in-memory

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Biologically detailed multi-compartment neuron simulation is essential for understanding brain functions and neural computation principles. However, executing these simulations on conventional von Neumann processors introduces severe memory access bottlenecks when solving the underlying Hines matrix equations. While analog neuromorphic hardware mitigates these data-movement challenges by mapping neuronal compartments to specific physical units. This compartment-centric mapping restricts structural flexibility, as rigid on-chip routing cannot accommodate diverse branching structures. To resolve these limitations, this work presents a connection-centric paradigm for biologically detailed neuron simulation based on a memristor computing-in-memory (CIM) architecture. By mapping the Hines matrix directly onto analog memristor crossbar arrays, the architecture represents arbitrary topologies without on-chip routing constraints. The system simultaneously achieves high energy efficiency through computing-in-memory and high flexibility through the mapping method. Moreover, to manage matrix sparsity across complex morphologies, a two-level sparse-aware processing methodology combining element-level reordering and block-level compression is developed, improving storage efficiency by more than 60%. The proposed paradigm is evaluated on a hardware platform integrating a digital core and memristor arrays. Experimental results demonstrate that the system successfully replicates critical neuronal functions, including passive dendritic propagation, coincidence detection, nonlinear feature binding, and network-level spike propagation. Compared to conventional hardware, the memristor-based system reduces energy consumption by up to 17.62 times and latency by up to 14.50 times, providing an efficient hardware solution for detailed brain modeling and next-generation artificial intelligence.

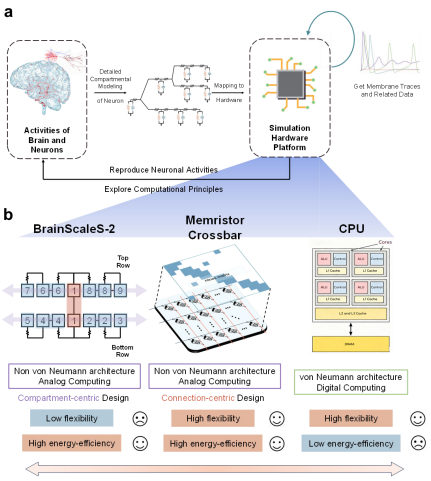


Figure 1. Simulation workflow of biologically detailed neuron and classification of simulation hardware. a Neurons in the brain were modeled as biologically detailed multi-compartment neuron models, deployed on a hardware platform for simulation, getting membrane potential traces and associated data over a specified time period. Simulations using detailed compartment model play an important role in reproducing the neuronal activities by extracting the underlying dynamics and exploring computational principles of the brain. b The spectrum of simulation hardware with different levels of flexibility and energy-efficiency. The proposed memristor crossbar-based simulator at the balance point of these considerations, which achieves high computing efficiency while maintaining high flexibility.

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A General Grey-Box Neural ODE Framework for Identifiable Memristor Modeling in Chaotic Circuits

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Memristor-based chaotic circuits are attractive for secure communication, hardware true-random-number generation, and neuromorphic computing. This work pursues two goals: (1) to realize a practical chaotic oscillator built around commercially available Self-Directed Channel (SDC) memristors [1, 2], and (2) to develop a physically interpretable, data-driven model of the embedded device, identified directly from the circuit's chaotic dynamics.

Conventional analytic models struggle to capture the nonlinear, history-dependent response of SDC memristors across operating conditions [3]. Data-driven Neural Ordinary Differential Equations (Neural ODEs) learn the internal-state evolution dx/dt = f(vm, x) from measured data. Our previous black-box realization used two free multilayer perceptrons ($\sim 10^5$ parameters) for the state rate and the conductance G(x); although accurate, it is weakly identifiable, since many distinct (parameter, initial-state) combinations reproduce the same trajectory.

We therefore introduce a general grey-box Neural ODE that retains the differentiable-solver pipeline but reduces the device to six physical parameters. The conductance uses the monotone backbone G(x) = x/Ron + (1−x)/Roff with x ∈ [0, 1], fixing the physical meaning of the latent state, and the state obeys a two-sigmoid law dx/dt = k·[(1−x)·sigmoid((vm−Von)/vt) − x·sigmoid(−(vm+Voff)/vt)], where the dimensionless rate k = τ/τ_mem relates the device timescale to the circuit timescale τ = Rref·C1, in which the ODE is integrated in dimensionless time for improved conditioning. Neither law is fully symbolic: a small bounded residual MLP additively corrects the rate dx/dt, and an optional bounded modulation h(x, vm), with |h| ≤ h_max, multiplicatively corrects the conductance as G(x, vm) = [x/Ron + (1−x)/Roff]·(1 + h). Both corrections are near-zero-initialized, recovering the symbolic device at initialization, so the physical structure dominates while the network only adjusts the symbolic prediction toward the measured response; positivity of the conductance preserves the pinched-hysteresis constraint im(vm = 0) = 0. The initial state is treated variationally: a bidirectional-GRU encoder maps a short voltage/current history to a logit-normal distribution, x_0 = sigmoid(μ + σ·ε), regularized by an annealed KL term, so that the imposed structure determines what x means.

A single shared device model is trained jointly across multiple operating points: by sweeping the digitally controlled potentiometer (AD5292) that sets R_3, several chaotic regimes were recorded and pooled, with R_3 entering each sample as a known parameter. This forces one physically consistent memristor to explain all regimes simultaneously and yields fitted parameters (Ron, Roff, τ_mem, Von, Voff, vt) with direct physical meaning rather than opaque network weights.

The oscillator uses a "jerk"-type topology [4], realized with SDC memristors on the assembled board shown in Fig. 1a, with the circuit diagram in Fig. 1b; Fig. 2 depicts the operation of the proposed grey-box Neural ODE.

This work was supported by the National Science Centre, Poland, grant no. 2024/53/B/ST7/03841.

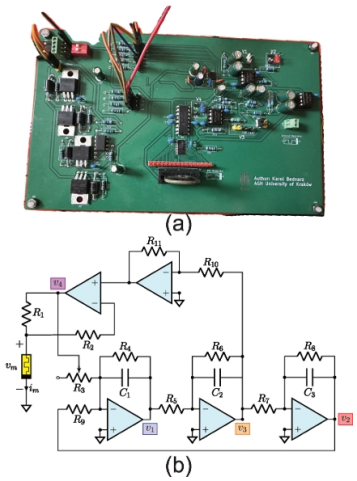


Figure 1. (a) Assembled memristor-based chaotic oscillator built around an SDC memristor with an AD5292 digital potentiometer; (b) circuit diagram of the ”jerk”-type oscillator topology.

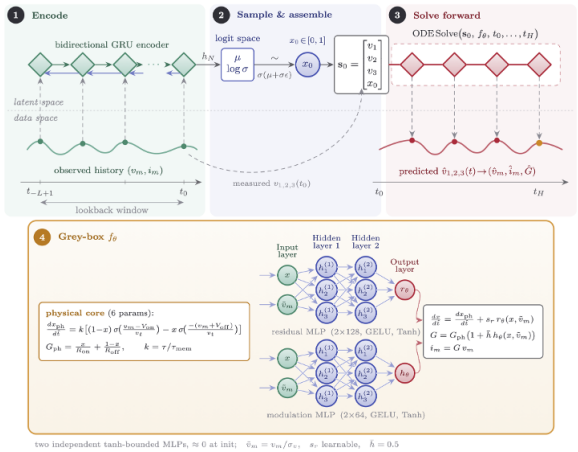


Figure 2. Computation graph of the proposed grey-box variational Neural ODE

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A Leaky-Integrate-and-Probabilistic-Fire Memristive Neuron for Probabilistic Spiking Neural Networks

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Probabilistic neural networks (PNNs) are critical for enabling uncertainty-aware artificial intelligence and generative modeling. To execute these models efficiently in hardware, the intrinsic stochasticity of memristive devices is increasingly leveraged for in-memory stochastic sampling, eliminating the need for area-intensive CMOS random number generators. While previous studies demonstrate that synaptic read and write noise can enable uncertainty-aware classification [1] and generative modeling [2], relying on synaptic stochasticity introduces a critical bottleneck. Forcing a single physical synapse to simultaneously encode both the deterministic weight (mean) and the probabilistic distribution (variance) inherently couples these parameters, severely complicating efficient training. Furthermore, the repeated device reprogramming required to drive continuous stochastic sampling incurs prohibitive energy and hardware overheads.

To overcome these limitations, stochasticity can be directly generated at the neuronal level. We utilize volatile diffusive memristors (DMs) with intrinsic stochastic switching characteristics to construct a leaky-integrate-and-probabilistic-fire (LIPF) neuron (Fig. 1a). In this architecture, a capacitor emulates the leaky integration of the membrane potential (Vm), while a DM in series with a transistor mimics the probabilistic opening of biological ion channels. The switching probability of the DM exhibits a natural sigmoid dependence on the applied voltage (Fig. 1b). Crucially, the series transistor is gated by the input signal, ensuring the DM experiences voltage and evaluates its probabilistic state only when an active input pulse is present (Fig. 1c). Consequently, the neuron's firing behavior becomes intrinsically probabilistic and dependent on Vm, closely resembling true biological firing dynamics rather than relying on rigid deterministic thresholds. Fig. 1d shows the neuron's responses under different numbers of integrated input pulses (Nint.) before firing, demonstrating the successful implementation of the LIPF functionality.

To validate its versatility, we integrate the LIPF neurons with a memristive synapse array to construct a probabilistic spiking neural network (PSNN) capable of both uncertainty-aware classification and generative modeling. For classification, the PSNN operates as the readout layer of a liquid state machine (PLSM; Fig. 2a). It achieves a 98.6% in-domain (ID) accuracy on the N-MNIST dataset while effectively distinguishing epistemic uncertainty between ID and out-of-domain (OOD) samples, yielding an AUROC of 0.92 (Fig. 2b-c). For generative tasks, the PSNN serves as the latent-space network within a spiking variational autoencoder (PSVAE; Fig. 2d), delivering image reconstruction performance on MNIST and F-MNIST datasets comparable to conventional SVAEs. Crucially, because stochastic sampling is handled intrinsically by the LIPF neurons rather than through redundant arrays of deterministic LIF neurons, the architecture reduces neuron and synapse counts by 3.4× and 20×, respectively (Fig. 2e), drastically minimizing hardware overhead.

In summary, we experimentally demonstrate the first hardware neuron capable of simultaneously realizing leaky integration and intrinsic probabilistic firing (Fig. 2f). By fundamentally decoupling stochastic generation from the synaptic memory array, the proposed LIPF architecture resolves the critical training and overhead bottlenecks of conventional memristive PNNs. Ultimately, this work provides a highly efficient, generalized hardware foundation for next-generation neuromorphic applications requiring complex probabilistic dynamics, including uncertainty-aware AI and spiking generative models.

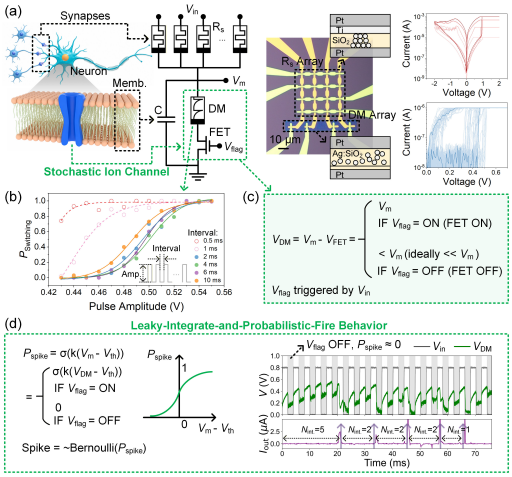


Figure 1. Structure and operating mechanism of the LIPF neuron. (a) Schematic and microscopic image of the LIPF neuron. (b) Sigmoid dependence of DM switching probability on input pulse amplitude. (c) Expression of VDM under Vflag gating control. (d) LIPF behavior of the neuron.

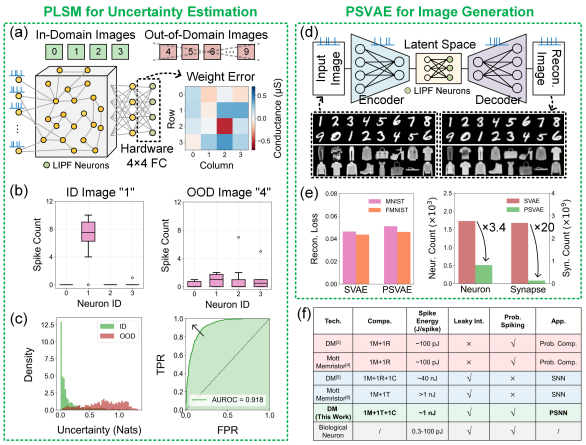


Figure 2. Applications of the LIPF-neuron-based PSNN. (a) Schematic of the PLSM and weight errors of the memristive synapses. (b) Experimental statistics of LIPF output spikes under repeated inference of ID and OOD samples. (c) Output entropy distributions of ID and OOD samples, and receiver operating characteristic curve and area under the curve (AUROC) for OOD detection. (d) Schematic of the PSVAE and generated images. (e) Comparison between SVAE and PSVAE in reconstruction loss, neuron count, and synapse count. (f) Performance comparison with existing memristor-based spiking neurons.

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A new simple and reliable memristive system for time-series data analysis

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Dynamic memristors represent a class of memristive devices defined by inherent time-dependent state dynamics. Unlike static (i.e. non volatile) memristors, which retain a fixed resistive state after stimulation, dynamic memristors exhibit transient conductance changes that decay over time [1]. This feature allows them to naturally emulate the fading memory effect whereby past inputs influence the current state but diminish in impact as time progresses. These devices that present short-term memory properties and complex nonlinearity are ideal for temporal computing tasks and especially attractive for physical reservoir computing [2].

In this work, we leverage the thermal inertia and temperature sensitivity of a resistive microheater to develop a new class of dynamic memristive systems with exceptionally low intrinsic variability. This makes the device particularly well-suited for reliable time-series data analysis. The microheater functions as a temperature-dependent resistive element: its resistance increases when heated by a current pulse and gradually decreases once the power is removed, thus enabling a fading memory effect. This new system is based on a Wheatstone bridge which integrates the microheater structure. It is elaborated with a simple two steps process on flexible polyimide substrate. The thermal inertia of the microheater is exploited for dynamic data storage and time-series data analysis. The electro-thermal system shows hysteretic Vout-Vin characteristics with ultra-low intrinsic variability and is able to dynamically code 16 different states. A proof of concept for digit recognition is finally achieved using this simple and reliable system.

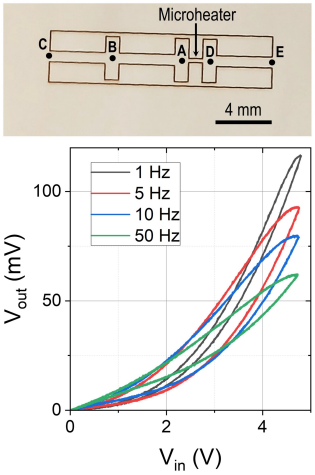


Figure 1. Photograph and Vout-Vin characteristic of the memristive system.

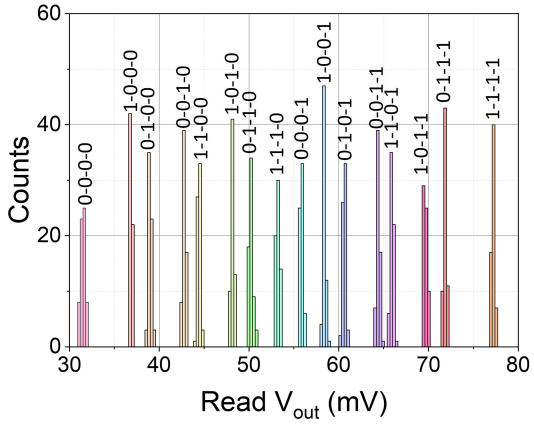


Figure 2. 4 bits coding showing the low cycle-to-cycle variability of the system.

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A Theoretical Framework for Optical Memristor-Based Cellular Neural Networks

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Emerging resistive switching devices (memristors) provide non-volatile, electrically programmable conductance states and exhibit synapse-like behavior, making them particularly attractive for bio-inspired computing systems. Optically sensitive memristors [1] further extend this functionality by enabling conductance modulation through controlled illumination, thereby allowing light to serve as a direct input modality. In particular, we consider a thin-film optical memristor based on a mixed layer of Si and Ge2Sb2Te5, which combines electrically programmable non-volatile conductance states with repeatable UV-induced conductance modulation (see Fig. 1). A key requirement for the proposed architecture is that the optically induced conductance change ΔG depends on the baseline conductance Gm allowing the same device to simultaneously perform optical sensing and implement a programmable synaptic weighting function (see Figs. 1 and 2). On the other hand, Cellular Neural Networks (CellNNs) constitute a spatially distributed, locally interconnected analogue computing paradigm that naturally supports massively parallel, continuous-time processing [2]. Inspired in part by the biological retina, CellNNs closely match the spatial organization of visual information and thus are especially well-suited for image processing and in-sensor computing applications [3].

In this work, we present a theoretical framework that combines optically sensitive memristors with CellNNs to realize an Optical Memristor CellNN (OM-CellNN) front end (see Fig. 2), in which incident light is directly converted into weighted analogue inputs at the pixel level. By exploiting the natural compatibility between optical sensing and CellNN processing, the proposed architecture could enable in-pixel, in-sensor computation towards energy-efficient edge AI systems capable of real-time visual signal processing.

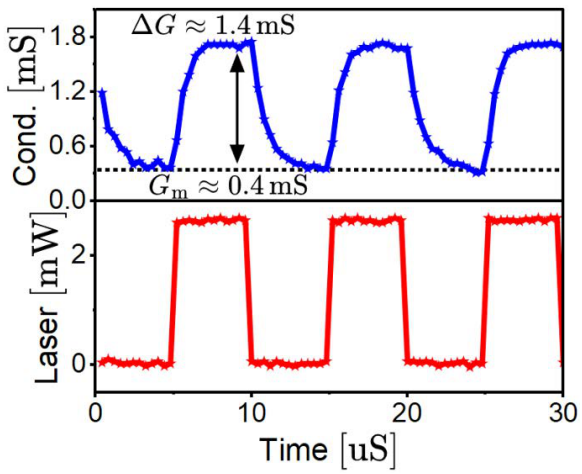


Figure 1. Schematic illustration of the conductance evolution under illumination, where incident light induces a conductance increase ΔG over a duration Δt, superimposed on the baseline conductance Gm.

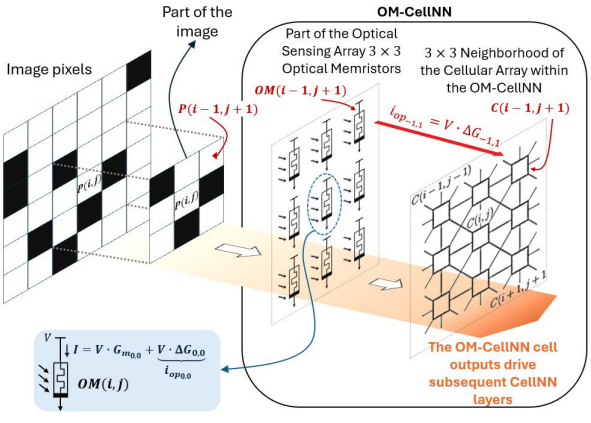


Figure 2. Architecture of the OM-CellNN front end.

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Design of a spiking error minimizing neuron in 130nm CMOS technology for self learning hardware neural networks.

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The broad field of neuromorphic computing presents itself as an attractive alternative to tackle the issues currently faced by conventional implementations of neural networks (NNs) in various artificial intelligence (AI) applications. In particular their heavy energy, resource, compute and data hungry operation and training could be addressed more efficiently. In this context, this work presents a mixed signal design of a low power spiking neuron (Fig. 1), as well as a memristor-based synapse design with the potential to allow the sidestepping of these problems, by enabling system-level implementations of NNs that approach the learning and operation processes from a computational neuroscience inspired angle.

This design takes inspiration from the predictive coding (PC) [1] theory of brain function as well as established control theory concepts. In PC, the global dynamics of a neural network evolve in such a way that a global free energy minimum, understood as the maximization of the correspondence between the internal model held by the neural network and the sensory data that it receives, can be reached by having neurons and synapses modify their behavior based only on their locally available information.

The possible discrepancy between the neural model and incoming sensory data is modelled at the neural level as an error, which takes the value of the difference between the actual spiking rate of the neuron and its expected activity value, understood as the sum of incoming currents. This error is minimized through a series of internal feedbacks (Fig. 2) by aligning the activity of the neuron with said expected value, resulting in dynamics beyond those found in standard Leaky Integrate-and-Fire (LIF) implementations, both at the neuron and at the network level, and that resemble those found in PC.

The constituent blocks of such a system will be presented, mainly neurons with the before mentioned dynamics, along memristive synapses that exploit the read-disturb phenomena observed in these devices [2] to autonomously update their conductances based on the activities of the neurons they link, following the weight update rules corresponding to PC in which errors are sent backwards. The presented results demonstrate the feasibility of implementing predictive coding dynamics in mixed-signal neuromorphic hardware through the combination of locally adaptive spiking neurons and memristive synapses.

This work was supported by the German Federal Ministry of Research, Technology and Space (BMFTR) under Grant 16ME1126K.

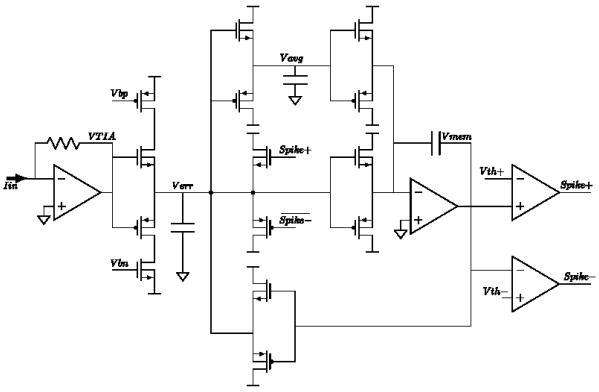


Figure 1. Schematic of the error minimizing neuron.

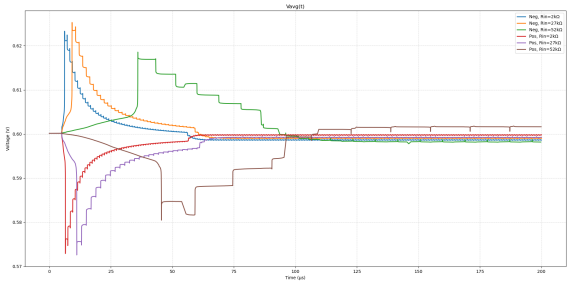


Figure 2. Vavg node under sustained voltage input for different synaptic and sign values. The values converge towards 600mV (chosen reference value).

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Electrically Tunable Physical Reservoir Computing on Two-terminal Devices

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Reservoir computing (RC) efficiently processes temporal data, but its tunability is critically constrained by the intrinsic relaxation timescales of the hardware. [1] Overcoming this limitation typically requires complex materials engineering or multi-terminal devices with additional optoelectronic stimuli. This work proposes a highly efficient, electrically tunable physical RC system utilizing simple two-terminal Pt/HfO2/TiN memristors. By modulating the base voltage amplitude between input voltage pulses, the device's intrinsic relaxation time is effectively extended by over two orders of magnitude. As illustrated in Fig. 1, this base voltage modulation achieves the high tunability and adaptability required for diverse timescales while preserving the structural simplicity of a conventional two-terminal architecture. This approach enables robust temporal data encoding for pulse intervals ranging from 0.14 to o 100 ms. The system's enhanced separability is experimentally demonstrated through Neuromorphic-MNIST classification. As shown in the top panel of Fig. 2, the tunable method maintains stable, high accuracy across diverse timescales, vastly outperforming conventional RC methods. Furthermore, the integration of a multi-cell grouped readout method significantly decreases readout layer size and latency with negligible accuracy degradation. Additionally, the predictive capability of the system is validated on chaotic Mackey-Glass time-series data. By employing multiple base voltage states to expand the reservoir capacity, a normalized root mean square error of 0.27 is achieved. The bottom panel of Fig. 2 highlights that this tunable RC approach achieves superior prediction accuracy utilizing significantly fewer training parameters than both software-based models and conventional RC architectures. This study presents a feasible and scalable pathway toward high-performance, tunable RC systems without relying on complex device engineering.

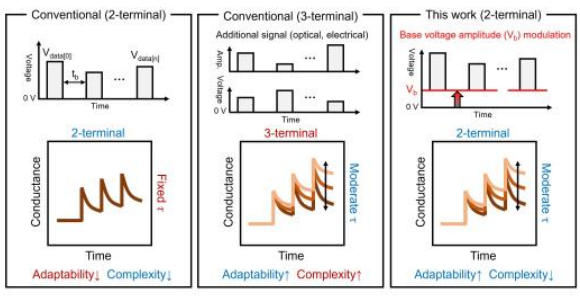


Figure 1. Schematic comparison of conventional reservoir computing approaches and the proposed method.

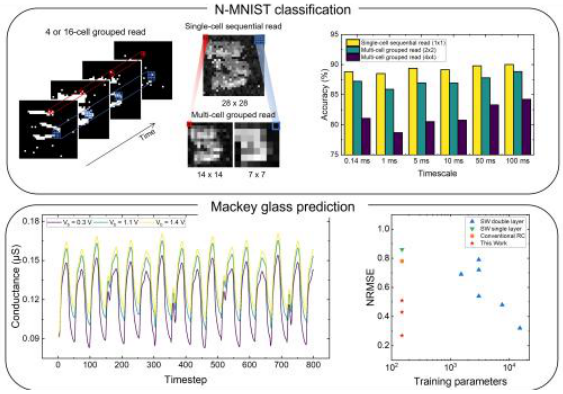


Figure 2. Performance evaluation of the tunable reservoir computing system in Neuromorphic- MNIST classification and Mackey-Glass time- series prediction.

References

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Experimental demonstration of scalable artificial neuron based on Ovonic threshold switch for spiking neural network applications

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Neuron plays a crucial role within the neural network in the generation, decision, and transmission of electrical spikes across the interconnected neurons. One of the key aspects of spike-based neural processing is its computational efficiency, which significantly reduces energy consumption compared to conventional counterparts. Their hardware implementation requires functional circuits for spike generation and communication; however, artificial neurons based on conventional CMOS face technical limits with respect to scalability, efficiency, and biological plausibility. Here, we investigate the artificial neuron behavior in Ovonic threshold-switching (OTS) device and its potential for spiking neural networks (SNN). Specifically, the intrinsic capacitance of OTS device originating from its two-terminal structure enables the formation of capacitor-less, scalable artificial neuron exhibiting leaky integrate-and-fire (LIF) behavior. Based on the designed OTS-based neuron circuit, various neural characteristics such as temporal dynamics and probabilistic characteristics are investigated to demonstrate its potential for biologically plausible artificial neuron. Furthermore, parametric analysis of OTS neuron depending on the circuit parameters are conducted to evaluate their effects on spike energy and frequency, showing spike energy of 1.53 nJ per spike and spike frequency of 100 kHz. Circuit simulations further demonstrate the potentials for performance improvements with sub-pJ spike energy. The findings establish the potentials for scalable, efficient artificial neurons for efficient SNN hardware.

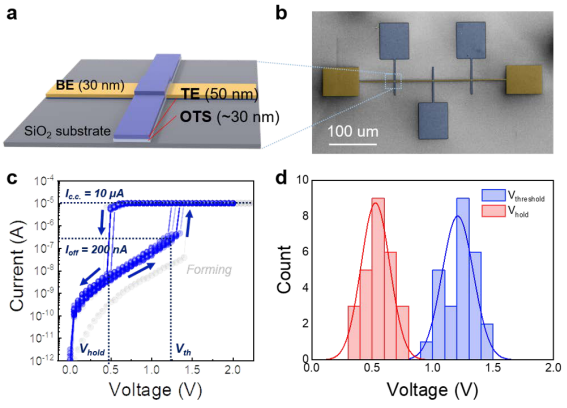


Figure 1. Device structure and electrical characteristics of Ovonic threshold switch. (a) Schematic of fabricated device, (b) SEM image of fabricated OTS device, (c) I-V characteristics of OTS device, and (d) variations of threshold voltage (Vth) and hold voltage (Vh).

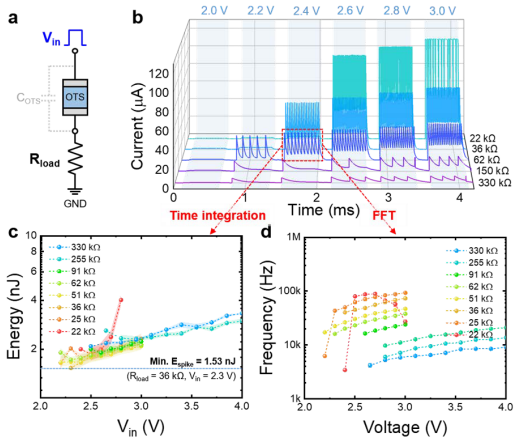


Figure 2. Parametric analysis of spike behavior of (a) OTS-based artificial neuron circuit, and (b) output spikes depending on load resistance and driving voltage. (c) Energy, (d) frequency evaluation of OTS-based artificial neuron.

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Feasibility study of a Parylene-based memristive capacitive Oscillator for Scalable Neuromorphic Hardware Architectures

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In this work, a proof of concept is presented for the use of a Parylene-based memristive layer in a neuromorphic circuit concept. Building on previous studies that demonstrated the suitability of the Parylene layer as a synaptic neuromorphic device [1], we now investigate its use as an oscillator. Specifically, we examine whether this layer, in combination with a capacitor and a current-limiting resistor, can be operated as a memristor-based relaxation oscillator. The goal is to generate self-sustained, neuromorphic action potentials solely by applying a DC voltage or defined voltage pulses, as used in spiking neural networks.

Current hardware approaches for biomimetic or neuromorphic artificial intelligence rely predominantly on complex transistor-based circuits to emulate biological functions. Alternative concepts that combine these functions within a single circuit element so far have been investigated almost exclusively using rare metal-oxide compounds [2], [3]. To date, no studies on comparable circuit elements based on polymer materials are known. Parylene-based layers are currently being explored exclusively as memristive synthetic synapses [4], [5].

The underlying operating principle is based on the voltage-dependent conductance change of the memristor. First, the capacitor charges via the circuit. Once the capacitor voltage reaches a material-specific threshold, the memristive Parylene layer switches into a highly conductive state. As a result, the capacitor discharges abruptly, generating a characteristic current pulse that mimics an action potential. Subsequently, the memristor returns to its high-resistance state, the capacitor charges again, and the process repeats periodically.

In the first step, the capacitor and current-limiting resistor were integrated into an external test setup. Experimental measurements demonstrated, for the first time, self-generated current pulses. The observed oscillatory behavior was reproducible but exhibited pronounced fluctuations in frequency and amplitude. These instabilities are attributed to material-specific and process-related variability of the Parylene layer. We discuss, which adjustments in material selection, layer design, and process parameters are required to achieve better control over the nonlinear dynamics of the system.

In future work, the memristor, capacitor, and resistor will be integrated into a multilayer system to realize neuromorphic action potentials within a compact circuit element. Such devices can serve as synthetic neurons and synapses and may form the basis for scalable neuromorphic architectures, particularly in the context of physical spiking neural networks (SNNs). Finally, the potential of Parylene-based memristive layers for neuromorphic computing is evaluated, and their role as a hardware alternative to complex transistor circuits exploiting intrinsically biomimetic, nonlinear dynamics is highlighted.

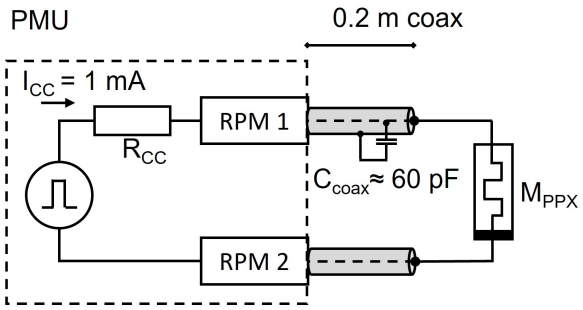


Figure 1. Schematic of the test setup for neural properties of a Parylene-based self-oscillating neuromorphic device

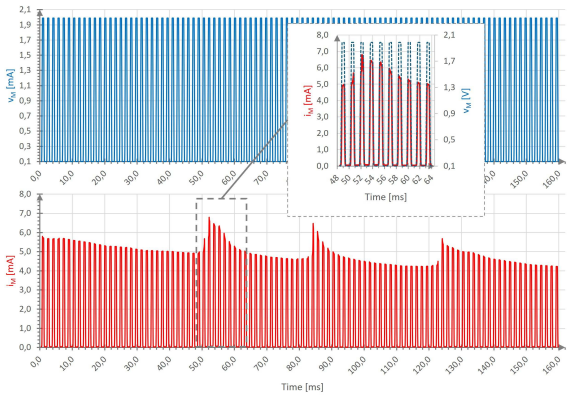


Figure 2. Current waveform (red) of the parylene-based layer in combination with the test setup for 100 voltage pulses (blue) with an amplitude of 2 V and a pulse duration of 1 ms

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Hybrid Analog–Digital Random Number Generator Based on Memristive Oscillators with Entropy-Seeding and FPGA Implementation

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This work presents the design and experimental implementation of a hybrid analog–digital random number generation architecture based on memristor-based relaxation oscillators and FPGA-based digital processing. The proposed system employs two Knowm Self-Directed Channel (SDC) memristors as analog entropy sources, whose nonlinear dynamics, intrinsic variability, and temporal fluctuations generate asynchronous oscillatory signals.

The conditioned oscillator outputs are combined through a digital XOR operation and sampled using a Nexys 4 DDR FPGA. Entropy is extracted from the pulse-width variations of a memristor-based relaxation oscillator and used to initialize a linear feedback shift register (LFSR), enabling entropy-assisted pseudo-random sequence generation through a lightweight digital architecture. Generated data was transmitted through UART communication at 115200 baud for external analysis.

Experimental evaluation was performed using multiple datasets containing 120,000 generated 8-bit values. The obtained histograms covered the complete output range from 0 to 255 and exhibited entropy-dependent inter-bin variability consistent with the stochastic behavior of the memristive oscillators and the asynchronous interaction between the analog and digital stages. Shannon entropy values were obtained, indicating a high degree of variability and broad utilization of the available output space. The presented architecture demonstrates the feasibility of using memristive devices as practical entropy sources for hybrid random number generation systems.

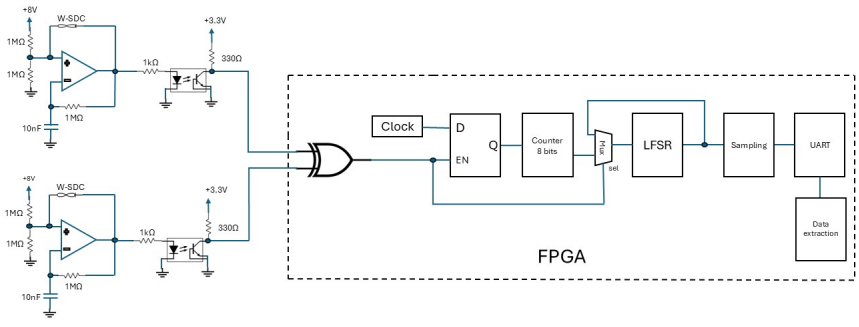


Figure 1. Proposed hybrid analog–digital random number generation architecture based on memristor-based relaxation oscillators and FPGA processing.

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Implementation of MIN and MAX fuzzy logic gates utilizing TaOx filamentary memristors

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Besides memory applications, memristive devices are also promising for logic and neuromorphic circuits [1, 2]. In particular, resistive switching-based devices are attractive for fuzzy logic, where information, unlike in traditional Boolean logic, is not restricted to only two states, but can acquire continuous values between 0 and 1. This makes fuzzy logic useful for processing imprecise data in cognitive computing, pattern recognition and information processing. Within this framework, the Min and Max functions are key operations corresponding to the intersection and union of fuzzy sets, respectively [3].

Filamentary memristors are especially suitable for hardware implementation of Min and Max functions because of their abrupt digital resistive switching [4]. Their sudden SET and RESET transitions allow well-defined changes between resistance states, which is advantageous for reliable evaluation of input levels. In this work, we study the implementation of fuzzy Min gates utilizing TaOx filamentary memristive devices. To achieve the well-defined threshold behavior required for the Min gate, the devices were prepared via two-step oxidation of tantalum to obtain a gradual oxygen gradient, as evidenced by XPS. Optimizing this preparation method is crucial, as the resulting oxygen profile within the oxide layer directly governs the formation of stable filaments enabling the desired abrupt switching.

Two configurations were investigated. The first one was based on two memristors connected in antiserial arrangement. The second one employed three memristors. In both cases the voltages were applied to the top electrodes, while the bottom electrodes were connected to a common node that was further linked through a high-resistance load to the ground. The behavior of these configurations was analyzed with respect to their ability to realize the Min and Max operations.

Our results show that TaOx filamentary memristors show promising potential for fuzzy Min and Max gates implementation, although further investigation is required to fully optimize their performance. The observed abrupt switching is an important prerequisite for this application, since it enables clear circuit response and stable operation.

Funded by the EU NextGenerationEU through the Recovery and Resilience Plan for Slovakia under the project No. 09I02-03-V01-00038 (Stephanik), and by the M-ERA.net project PhotoPrint.

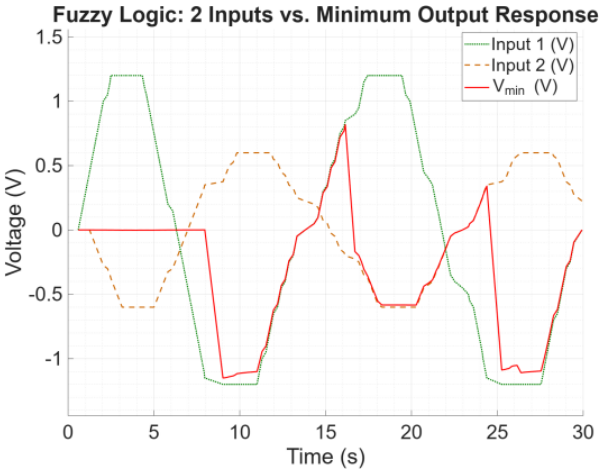


Figure 1. Voltage response of the implemented two-input fuzzy Min-gate configuration. The solid red curve highlights the output voltage dynamically tracking the minimum envelope of the two distinct time-varying input signals.

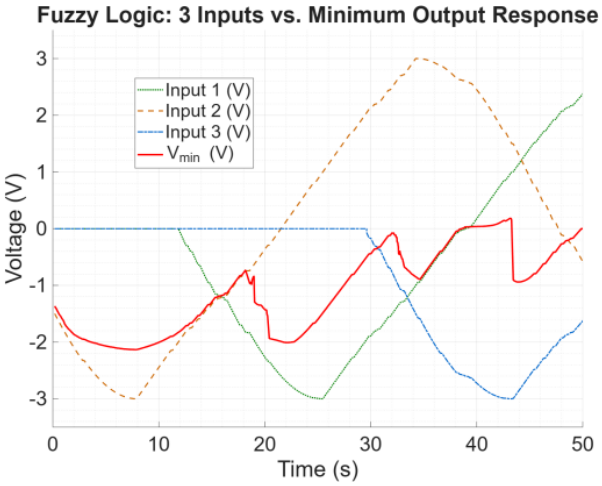


Figure 2. Voltage response of the implemented three-input fuzzy Min-gate configuration. The solid red curve highlights the output voltage dynamically tracking the minimum envelope of the three distinct time-varying input signals.

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In-Memory Computing Inspired Framework for Early Soybean Leaf Disease Recognition

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Early and accurate diagnosis of crop diseases is essential for ensuring agricultural productivity, minimizing yield losses, and reducing the excessive use of pesticides. Soybean, one of the world's most important oilseed and protein crops, is highly susceptible to a variety of foliar diseases that adversely affect crop quality and yield. Conventional disease assessment methods rely heavily on manual inspection by experts, which is often time-consuming, subjective, and inaccessible to farmers in remote regions. Recent advances in artificial intelligence have enabled automated plant disease detection; however, the deployment of deep learning models on resource-constrained edge devices remains challenging due to computational complexity, memory requirements, and energy consumption. To address these limitations, this work presents an **in-memory computing inspired framework for early soybean leaf disease recognition**, integrating a discrete wavelet transform (DWT)-enabled memristive crossbar array (MCA) with lightweight deep learning models for efficient and accurate field-level disease diagnosis.

The proposed framework leverages the intrinsic parallelism and analog computing capabilities of memristive crossbar arrays to perform image preprocessing operations in a highly energy-efficient manner. Specifically, the DWT-enabled MCA is employed as a feature-preserving image decomposition and reconstruction module, enabling efficient compression while retaining disease-relevant visual characteristics. The reconstructed images exhibit high structural fidelity, achieving peak signal-to-noise ratio (PSNR) values exceeding 20 dB along with high structural similarity index (SSIM) scores. These characteristics ensure that critical disease symptoms, including lesion boundaries, discoloration patterns, and texture variations, are preserved for subsequent machine learning analysis.

Following preprocessing, the framework utilizes a two-stage deep learning pipeline optimized for edge deployment. In the first stage, a YOLOv8-based object detection model localizes soybean leaves from complex field images containing varying backgrounds, illumination conditions, and occlusions. The detected leaf regions are then passed to a MobileNetV2 classifier that categorizes samples into seven major soybean disease classes, including frogeye leaf spot, target spot, yellow mosaic disease, and healthy leaves. The lightweight architecture significantly reduces computational overhead while maintaining high classification performance. Both models are converted and deployed using TensorFlow Lite, enabling real-time inference on Android smartphones with low latency and reduced energy consumption.

To facilitate practical adoption in precision agriculture, the proposed system is implemented as a user-friendly Android application featuring multilingual support, including English, Hindi, and regional languages. Beyond disease identification, the application provides disease-specific management recommendations, preventive measures, and treatment guidelines, thereby supporting informed decision-making by farmers and agricultural extension workers. This integration of intelligent diagnostics and actionable advisory services contributes to the development of accessible smart farming solutions.

Experimental evaluation demonstrates the effectiveness of the proposed framework, achieving a classification accuracy of 95.70% across eight soybean leaf categories. The DWT-enabled MCA preprocessing stage improves feature quality and classification reliability while reducing computational requirements, highlighting the potential of memristive in-memory computing concepts for edge-based agricultural intel-

ligence. The proposed approach establishes a pathway toward energy-efficient, scalable, and deployable crop health monitoring systems, bridging the gap between emerging memristive computing technologies and real-world precision agriculture applications.

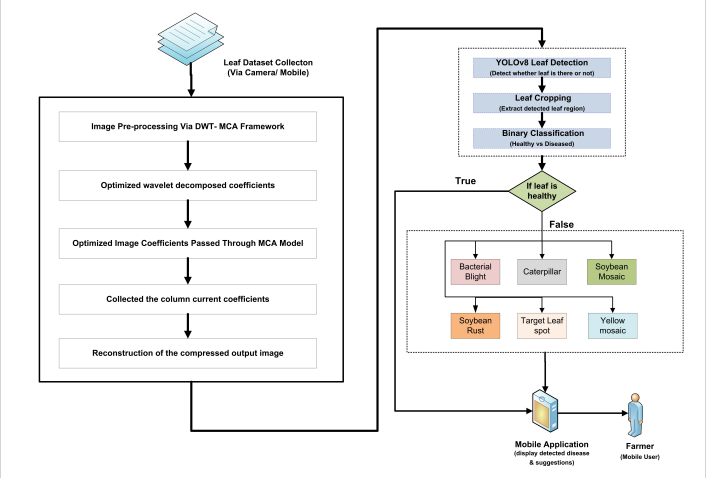


Figure 1. Flowchart of the proposed framework for the soybean leaf disease detection.

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Investigation on the Impact of Memristive Device Variability on Uncoupled Memristive Cellular Nonlinear Networks

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Conventional von Neumann architectures suffer from a fundamental bottleneck arising from the physical separation of memory and processing units. Memristive Cellular Nonlinear Networks (M-CellNNs) offer a promising path to mitigate this limitation by enabling in-memory computation with enriched nonlinear cell dynamics. However, the practical viability of M-CellNN hardware implementations depends critically on their robustness to the intrinsic variability of memristive devices, a question that has so far been addressed only at the simulation level, without grounding in experimentally measured device statistics from a physical M-CellNN cell.

In this work, we present a variability-aware investigation of an uncoupled M-CellNN implementing EDGE detection, combining physical breadboard experiments with SPICE-level array simulations calibrated to experimental data. In the M-CellNN cell architecture, the memristive device is integrated in parallel with the resistor and capacitor of the core RC circuit, enriching the cell dynamics with a voltage-dependent nonlinear conductance [1]. Five nominally identical Pt/HfO_2/TiO_x/Ti/Pt (HOTO) valence change mechanism (VCM) devices were individually integrated into an M-CellNN breadboard cell, and their transient responses under the worst-case local rules of the EDGE detection template were experimentally characterized using a Keithley 2611A SMU and a Tektronix DPO7254 oscilloscope. The measurements reveal D2D variability levels that significantly exceed those assumed in prior simulation studies, providing a more realistic baseline than previously reported, as shown in Fig. 1. The experimentally extracted variability statistics were used to calibrate the physics-based JART VCM v1b compact model in Verilog-A within a Cadence simulation environment. Cycle-to-cycle variability had a negligible impact on system-level accuracy since each cell undergoes only a single switching operation per image-processing task. D2D variability, by contrast, accumulates across the array and directly affects transient behavior and steady-state convergence, making it the dominant source of performance variation. Variability-aware SPICE-level simulations of a 16×16 M-CellNN array were performed, with each cell assigned independently sampled physical model parameters drawn from a truncated Gaussian distribution fitted to the experimental data.

Despite substantial stochastic fluctuations, the network achieves 100% pixel-level EDGE detection accuracy, with all 60 true edge pixels correctly identified and no spurious detections. This robustness is inherent to the uncoupled architecture, since each cell evolves under its own local rule without dynamic inter-cell state feedback, so any variability-induced error remains spatially isolated and cannot cascade across the array. The analysis was further extended to passive component variations. With a global RC deviation of ±20% and a local mismatch of ±2%, and accounting for D2D variability, 100% accuracy is maintained in both cases, as summarized in Fig. 2. These findings establish the uncoupled M- CellNN as a viable candidate for monolithic integration in neuromorphic and in-memory computing systems, and demonstrate that experimentally calibrated variability-aware simulation is essential for realistic robustness assessment. Tolerance boundaries under more extreme mismatch conditions are further

investigated through variability-aware simulations, with tolerance-aware template design strategies for next-generation M- CellNN implementations planned as future work.

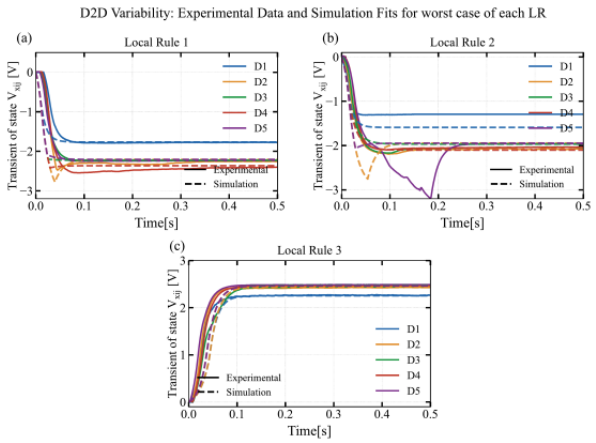


Figure 1. D2D variability-aware transient response of V_{xij} for local rules 1–3. Five VCM devices were measured (solid lines, C_X= 10 µF) and fitted with SPICE simulations (dashed lines)

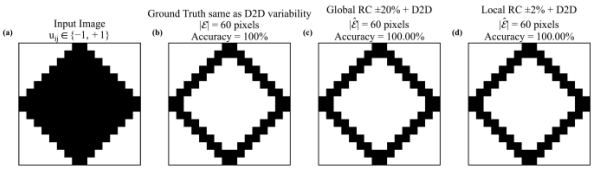


Figure 2. EDGE detection in the 16×16 M-CellNN under different variation scenarios: (a) input image, (b) ground truth / D2D variability, (c) global RC ±20% + D2D, (d) local RC ±2% + D2D. All cases achieve 100% accuracy with no spurious or missed edge pixels.

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Live Demo: Non-Frontal Face Recognition Using GANs and Memristor-Based Classifiers

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Face recognition systems have advanced significantly through deep learning techniques, achieving strong performance in a wide range of scenarios. However, these approaches typically involve substantial computational cost, which limits their deployment on resource-constrained edge platforms such as drones. This is particularly challenging in real-world aerial and mobile sensing applications, where facial images are often captured from non-frontal viewpoints, leading to degraded recognition performance. These conditions require methods that can handle pose variations effectively while remaining computationally efficient for size, weight, and power (SWaP)-constrained systems.

Memristor-based neuromorphic systems have recently attracted interest as a promising option for edge AI applications, owing to their potential for efficient and scalable computation inspired by neural processing principles. In parallel, generative adversarial network (GAN)-based models can be used to mitigate pose variation by reconstructing more frontal facial representations from non-frontal inputs. Based on these ideas, we previously proposed a hybrid framework that combines a lightweight GAN-based face reconstruction unit (FRU) for pose frontalisation with a memristor-based face classification unit (FCU) for neuromorphic recognition [1].

In this work, we present an end-to-end implementation of this framework through an interactive live demonstration. The system allows users to capture non-frontal facial images using a camera, observe the frontalisation process performed by the GAN-based FRU, and view the corresponding recognition results produced by the memristor-based FCU.

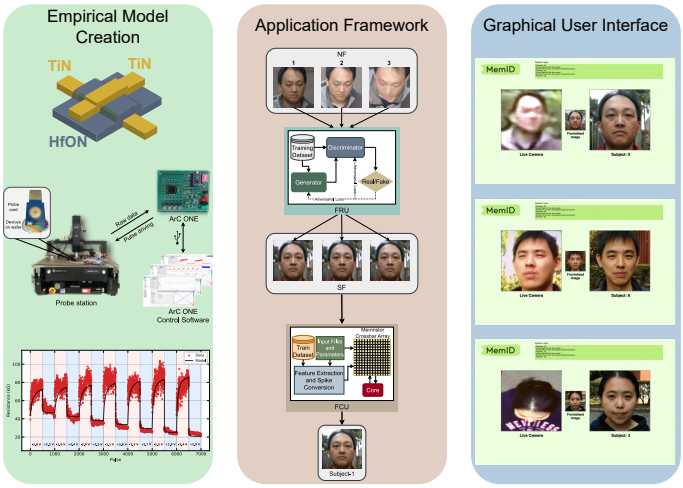


Figure 1. End-to-end application pipeline

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Machine Learning for Memristive Device Modeling: Automated Parameter Fitting for the Dynamic Memdiode Model

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The accurate characterization of memristive devices, particularly RRAM, is essential for advancing both device-level optimization and neuromorphic engineering. The Dynamic Memdiode Model (DMM) has proven highly effective in this regard, providing a computationally efficient foundation capable of simulating both isolated RRAM devices and large-scale, RRAM-based artificial neural networks [1]. However, the manual extraction of DMM parameters is a time-consuming process that lacks scalability. Recent approaches, such as those utilizing Convolutional Neural Networks (CNNs) to map visual representations of I-V curves to model parameters, have demonstrated the potential for automated fitting [2]. While promising, these methods rely on the transformation of experimental data into standardized image formats, which introduces additional preprocessing overhead and potential information loss.

In this work, we propose a novel machine learning framework designed to automate the parameter extraction of the DMM by operating directly on raw experimental data. By transitioning from image-based inference to direct sequence processing of voltage-current time-series data, we aim to eliminate the necessity for visual transformation and improve the fidelity of the parameter fitting process. This work is a collaborative effort between machine learning and materials science laboratories, uniting expertise in neural architecture design with high-resolution, experimental device characterization data to ensure the model is validated against real-world switching dynamics.

A central challenge in processing raw text-based device data is the lack of uniformity across experimental trials. This variability can manifest in several forms, such as differences in sampling rates, temporal scales, voltage ranges or initial internal ion vacancy states. To address this, we investigate specialized preprocessing pipelines and architectural innovations capable of handling variable-length sequential inputs. We explore the implementation of robust normalization techniques and sequence-aware deep learning architectures, such as Recurrent Neural Networks (RNNs), Transformers, or specialized pooling layers, to ensure consistent feature extraction regardless of the input format.

Our primary objective is to develop an end-to-end pipeline that maps raw, non-uniform measurement data directly to accurate model parameters, thereby reducing the time and computational cost associated with device characterization. We intend to compare the performance of our proposed sequence-based methodology against established image-based CNN approaches [2] to quantify improvements in computational efficiency. This research aims to provide a robust, scalable, and automated fitting procedure, offering a critical tool for researchers and engineers tasked with modeling complex resistive switching phenomena and accelerating the iteration cycles in materials development.

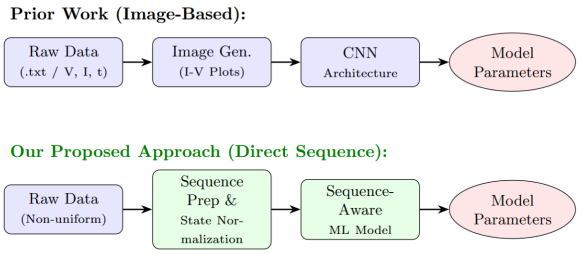


Figure 1. Comparison between the image-based fitting framework and our proposed direct sequence-based framework.

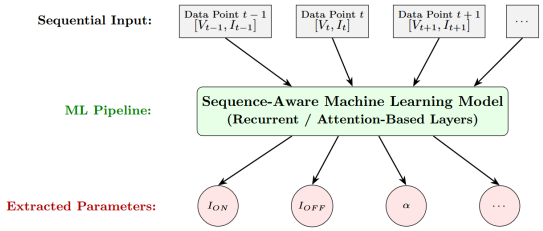


Figure 2. Structural layout of the proposed sequence-to-parameter ML model, mapping raw, temporal voltage-current vectors directly to extracted Dynamic Memdiode Model parameters.

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Memristive Bio-Sensors for Highly-Sensitive Bio/Chemical Detection Applications

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Parkinson's disease affects over 8.5 million people worldwide and is projected to double in prevalence over the next 25 years [1]. Because symptoms typically appear only after more than 60% of dopaminergic neurons are lost, diagnosis occurs late, highlighting the need for early detection technologies.

Meanwhile, memristive devices have emerged as a powerful tool in bio/chemical sensing due to their unique properties. Unlike traditional sensors, memristors offer the advantages of high sensitivity, scalability, reconfigurability, and low-power consumption. These emerging technologies, coupled with biological processes, opened new perspectives in the role of bio-inspired sensors introducing a versatile paradigm for label-free and ultra-sensitive bio/chemical sensing [2].

We incorporate bio-functionalized memristive elements – whose resistance depends on the history of applied charges, employed as electrochemical biosensors for the detection of biomarkers below and within the fM range. This property allows for detection of even small biomarker variations, with current and previous relevant works [3,4] showing high sensitivity, which is crucial to detect the early variations in biomarkers. The sensing mechanism is based on the monitoring of the resistive state shifts depicted when charged bio/chemical residues are uptaken on the device surface, and dependent on the type and the concentration levels of the biomarkers. The implementation of a tailored surface chemistry and bio-recognition elements ensures the specificity of the sensors thanks to the high affinity of the receptors to recognize their specific target and not structurally similar molecules. Overall, these memristor-based sensing devices ultimately lead to a label-free, highly-sensitive and high-specific bio-detection system capable of sensing a wide range of biomarkers providing an early-stage detection of the medical condition.

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Memristive Synaptic Circuit Configurations under Device Variability and Nonlinear Effects

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Developing hardware-based synaptic circuits that are both resilient and adaptive is key to enabling bio-inspired processing in emerging application areas such as 6G communications, IoT, and edge computing [1]. Non-volatile memristors, with their data-retention capability and low power consumption, are well-suited for reproducing synaptic dynamics [2,3]. When integrated as synapses within Cellular Neural Networks (CellNNs) they form Memristor-CellNNs (M-CellNNs), whose unique electrical properties can improve network performance and efficiency [4]. In practice, hardware implementations inevitably introduce non-idealities, including device-to-device variability, nonlinear conductance behavior, and asymmetric switching characteristics. These effects may reduce network reliability, yet they can also give rise to new functionalities. Characterizing and modeling their influence on M-CellNN dynamics is therefore important for both system assessment and the identification of potential hardware-level benefits [5].

In this work, we investigate the behavior of different synaptic circuit topologies based on Valence Change Mechanism (VCM) memristors, when being subject to hardware non-idealities. Four circuit configurations are studied: (I) a digital reference synapse, (II) a single-memristor synapse, (III) a two-memristor differential-output synapse, and (IV) a two-memristor inverted-input synapse, see Fig. 1. During a network operation, the voltages applied to the synapses remain low, so the internal state of the memristors does not change and the desired weight is constant. However, under realistic conditions, hardware non-idealities, specifically nonlinearities, asymmetries, and device-to-device variability, become important factors that affect network performance. To examine this, we investigate conductance at read voltage to each synaptic circuit and study how the conductances and the final weights are affected. Fig. 2 presents the normalized conductance (G_Mem/G_Ref) or desired weights as a function of applied voltage for three cases (Q = 8, Q = 2, Q = -1), which corresponds to a combination of the inner states of the memristors within the given topology. The digital reference synapse (I) produces a flat, state-independent response across all charge states. In contrast, synaptic memristive topologies (II–IV) exhibit nonlinear and asymmetric characteristics. The final weight in cases II and III decreases with a negative applied voltage and increases with a positive voltage and for case IV vise versa. The intensity and behavior of these phenomena depend on both the circuit topology and the desired weight deviations from the ideal are most significant in the case Q = 2. All three synaptic configurations exhibit the greatest deviations from the ideal case at this weight, identifying it as the worst operating synapse. At Q = 8, the effect of the non-idealities is less pronounced. At Q = -1, the weight values shift further. In this case, the synapse with two memristors and an inverted input exhibits the most significant deviation among all topologies. These non-ideal synaptic weights propagate through the M-CellNN and may shift the network's equilibrium states. The results highlight the critical role of synaptic circuit design in the performance of the M -CellNN and demonstrate that careful selection of the synaptic topology ais necessary for advanced bio-computing applications.

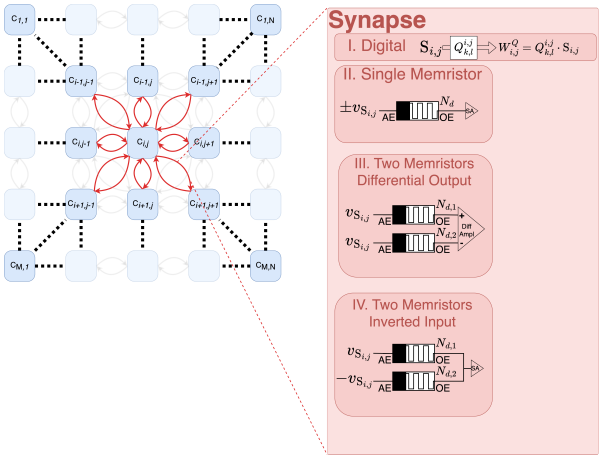


Figure 1. Schematic representation of the four investigated synaptic circuit topologies: (I) digital reference synapse, (II) single-memristor synapse, (III) two-memristor differential-output synapse, and (IV) two-memristor inverted-input synapse.

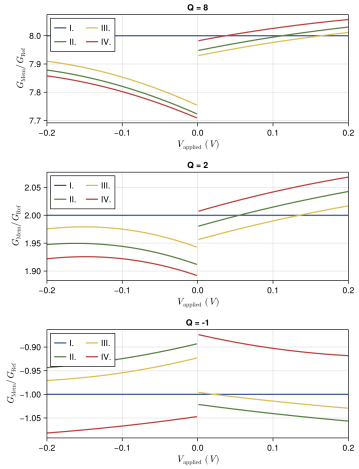


Figure 2. Normalized synaptic conductance (weight) as a function of applied voltage for different synaptic topologies. The plots compare the behavior across three cases (Q=8, Q=2, and Q=1), highlighting the nonlinear and asymmetric characteristics induced by hardware non-idealities.

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Neurocontroller Based on an Analog 1R Memristor Crossbars

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Memristors are emerging electronic devices with significant potential for neuromorphic hardware. One of the most widely discussed applications is the implementation of memristors as weights in neural network architecture. When arranged in crossbar structures, memristors can perform analog vector matrix multiplication with high parallelism and potentially low energy consumption [1]. In our previous research, we developed analog memristors based on Ni/HfO2/TiO2/TiN layers. These memristors has high nonlinear current–voltage behavior that can suppress sneak-path currents in crossbar arrays, which allow us to implement these memristors in 1R crossbars without any additional selector [2]. However, this nonlinearity makes the weight dependent on the applied voltage which might be considered as disadvantage.

In this work, we investigate the capability of these nonlinear analog memristors to realise artificial neural network (ANN) used as a controller. Conventional control systems are commonly based on closed-loop feedback structures using controllers such as proportional, Integral, derivative (PID) controller. Neural network based controllers (neurocontrollers) may provide advantages when controlling nonlinear systems or systems with complex dynamics. To evaluate the proposed approach, we firstly developed a compact model of our analog memristors, based on the existing Yakopcic memristor model [3]. Defined compact model was integrated into the neural network architecture to represent the electrical behavior of the memristive weight. The resulting memristor based neurocontroller was then simulated in Matlab and its network parameters were optimized using a neuroevolutionary algorithm.

The proposed memristor based neurocontroller is evaluated on three systems with progressively more complex dynamics. The main objective is to provide a proof of concept demonstrating that a neural structure composed of nonlinear memristive synapses can be trained and applied to closed loop control tasks. Its performance is evaluated against a multilayer perceptron (MLP) based neural network controller and a PID controller.

As an initial case study, the proposed neurocontroller was used to control speed of a small DC motor. The controller used three input signals: the control error, the derivative of the system output, and the system output. Architecture of used neurocontroller consisted of one hidden layer with five neurons and one output neuron representing the motor input voltage as shown in Fig. 1. The results presented in Fig. 2 demonstrate that the Memristor based neurocontroller successfully controlled the motor speed and achieved performance comparable with the MLP based ANN and PID controllers.

To identify the potential advantages and limitations of the memristor-based approach, additional systems with more complex dynamics are currently being investigated. Their evaluation will focus on control accuracy, stability, robustness, and suitability for practical control applications. The presented study will therefore provide an initial assessment of whether nonlinear analog memristors can serve as functional synaptic elements in trainable neuromorphic controllers.

Acknowledgement: Funded by the EU NextGenerationEU through the Recovery and Resilience Plan for Slovakia under the project No. 09I02-03-V01-00038 (Stephanik), and by the M-ERA.net project PhotoPrint and by the slovak grant agency APVV-22-0169.

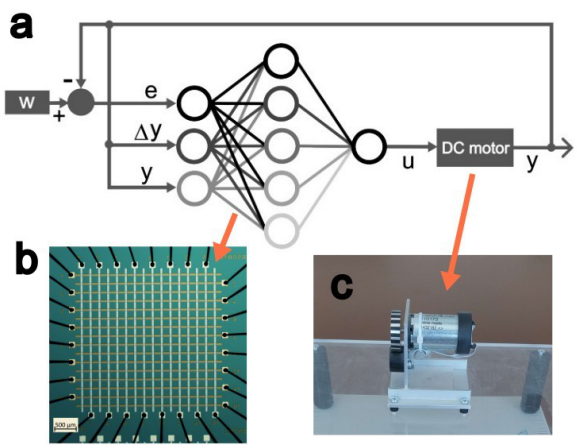


Figure 1. (a) Closed loop control system with the proposed neurocontroller, (b) memristor crossbar structure, and (c) controlled DC motor.

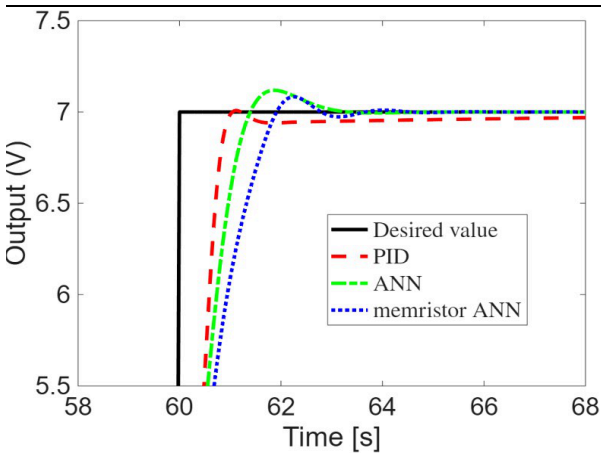


Figure 2. Comparison of PID, conventional ANN, and memristor based ANN controllers for DC motor speed control.

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Neuromorphic Sleep Monitoring with RRAM-based In-Memory FIR-Hilbert Preprocessing and SNN Inference

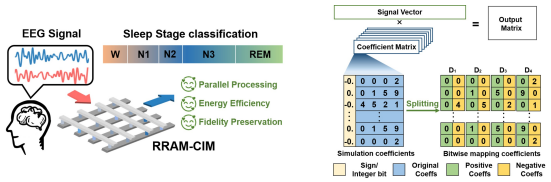
Jingyi Chen[1], Xinxu Lin[1], Zhicheng Li[1], Zihan Xu[1], Jingsong Zhang[1], Fangduo Zhu[1],Yiwen Zhu[1], Siyuan Ouyang[1], Jinhao Liang[1], Xinming Shi[2], Xumeng Zhang[1], Qi Liu[1]

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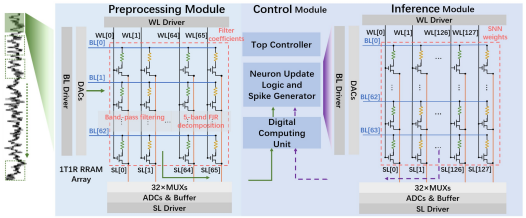
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Continuous sleep monitoring is important for personalized healthcare, but EEG-based sleep-stage classification remains challenging for wearable and edge devices due to stringent power, latency, and area constraints. Conventional digital pipelines typically separate signal preprocessing, memory access, and neural inference, resulting in substantial data movement during long-term operation. To address these challenges, we present an RRAM-based computing-in-memory (RRAM-CIM) neuromorphic sleep monitoring system that integrates EEG signal preprocessing, spike encoding, and spiking neural network (SNN) inference within a unified memristive hardware framework. The proposed system maps FIR-Hilbert preprocessing directly onto RRAM crossbar arrays using analog vector-matrix multiplication. Raw EEG signals are processed by a band-pass FIR filter and a multiband FIR filter bank to extract subband activities associated with δ, θ, α, β, and γ rhythms. Hilbert transform is then applied to obtain temporal envelope features, which are converted into sparse spike events by level-crossing encoding and subsequently processed by an RRAM-based SNN classifier.

To preserve preprocessing fidelity under RRAM device non-idealities, including conductance drift and read noise, a Split Kernel Value Mapping (SKVM) strategy is developed to decompose FIR-Hilbert coefficients with a wide dynamic range into fine-grained differential conductance representations. This mapping strategy enables high-fidelity coefficient deployment and mitigates signal distortion before spike-domain inference. Fabricated in a 180 nm process, the proposed RRAM-CIM system demonstrates both accurate signal processing and energy-efficient inference. The SKVM-based preprocessing achieves strong hardware/software consistency, with envelope correlation exceeding 0.995. The on-chip RRAM-CIM SNN obtains 85.3% sleep-stage classification accuracy, with only 3.1% degradation from the software baseline. The system achieves a power consumption of 4.15 μW/sample, corresponding to an estimated 3.98 mJ energy consumption for an 8-hour overnight monitoring session. This work provides a compact, accurate, and energy-efficient hardware foundation for always-on edge sleep monitoring, highlighting the potential of memristive systems for neuromorphic biomedical intelligence.

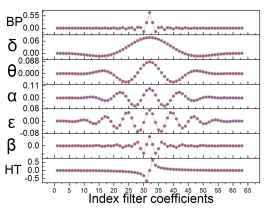


(a) RRAM-CIM EEG Sleep Monitoring (b) SKVM-Based Coefficient Mapping

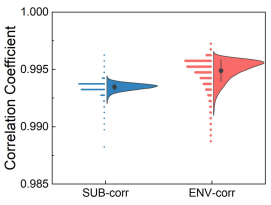


(c) In-Memory Preprocessing and SNN Inference

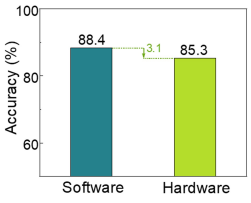
Figure 1. Overview of the RRAM-CIM sleep monitoring system, including EEG-based sleep staging, SKVM-based coefficient mapping, and integrated in-memory preprocessing/SNN inference architecture.



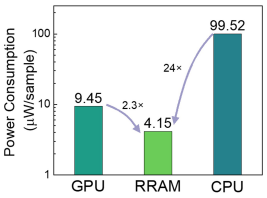
(a) SKVM Mapping Fidelity



(b) RRAM Preprocessing Correlation



(c) On-Chip Sleep-Staging Accuracy



(d) Power Consumption Comparison

Figure 2. Experimental results showing SKVM mapping fidelity, high RRAM preprocessing correlation, 85.3% on-chip sleep-staging accuracy, and 4.15 μW/sample power consumption.

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Noise and Accuracy Analysis of RRAM-based Analog Matrix Equation Solving Circuit

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Driven by the unprecedented growth of computational data and the rapid advancement of artificial intelligence (AI), traditional digital computing is increasingly constrained by the slowdown of Moore's Law and the von Neumann bottleneck [1]. In response, RRAM-based analog matrix computing (AMC) has emerged as a promising paradigm. By operating in the continuous time domain, AMC directly utilizes physical analog quantities to solve complex matrix equations, a fundamental operation in linear algebra, in one step [2]. Unlike traditional digital computing that solves matrix equations with a computational complexity O(N3), AMC can achieve constant-time complexity, i.e., O(1), thereby facilitating high-performance computing systems.

Despite its significant computational advantages, AMC faces critical challenges in computational accuracy, particularly for large-scale applications. Analog systems are inherently susceptible to random noise and hardware non-idealities. System accuracy is often limited by factors such as the limited resolution of data converters, operational amplifier (OA) non-idealities and RRAM programming errors. Furthermore, the scale and condition number of the matrix being solved can significantly affect the solution accuracy. Consequently, even small signal perturbations may substantially degrade the quality of the computed results. Although extensive studies have investigated noise modeling for conventional matrix-vector multiplication (MVM) and digital in-mmeory computing (IMC) system [3-4], a comprehensive noise analysis framework for AMC circuits specifically designed to solve systems of linear equations remains largely unexplored.

In this work, we present a comprehensive noise analysis framework for AMC circuits dedicated to solving systems of linear equations. As illustrated in Fig. 1, we derive the overall system noise from the underlying circuit transfer characteristics and model its contributions through four categories of noise sources, quantitatively characterizing each source together with its corresponding noise gain. In addition, we introduce the concept of inherent error (IE) to explicitly capture the unique impact of RRAM programming inaccuracies. The proposed model is validated through circuit-level SPICE simulations. Using this framework, we quantitatively evaluate the effects of matrix size, condition number, and RRAM conductance variation on overall computational accuracy (Fig. 2). These systematic results provide practical design guidelines for developing robust RRAM-based AMC systems and lay the foundation for high-precision scientific computing and advanced neural network accelerators.

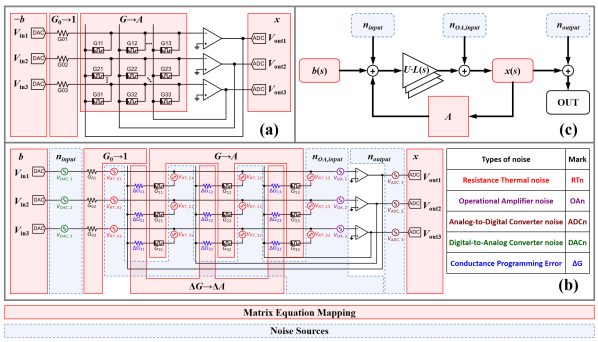


Figure 1. a, Ideal model of AMC. b, Non-ideal model of AMC. c, Block diagram of the non-ideal circuit as a control system.

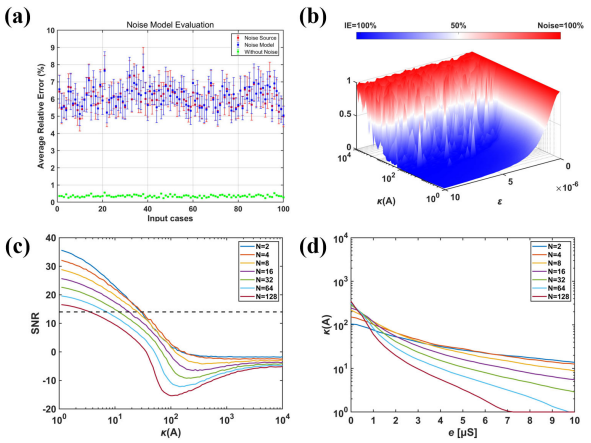


Figure 2. a, Noise model validation between the SPICE model and the proposed model. b, Impact of matrix condition number and programming error on the percentage of random noise and IE. c, Impact of matrix size and matrix condition number on the SNR. d, Impact of matrix size and programming error on the critical matrix condition number.

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Noise-Assisted Variability-Tolerant IMPLY Logic Using Memristive Devices

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Memristive devices are promising building blocks for in-memory computing [1], where logic operations can be performed directly on stored resistance states. Among the most established stateful logic primitives, material implication (IMPLY) is particularly attractive because, together with the FALSE operation, it forms a computationally complete logic basis [2]. However, the reliability of memristive IMPLY logic is strongly limited by cycle-to-cycle and device-to-device variability. A fixed programming pulse may fail to switch slow devices while unintentionally disturbing fast devices that should remain unchanged.

In this work, we investigate whether deliberately added zero-mean voltage noise can improve the reliability of variability-limited memristive IMPLY logic. The approach exploits stochastic resonance: due to the strongly nonlinear switching kinetics of memristive devices, small voltage fluctuations can enhance the effective switching rate of slow cells without equally affecting all logical cases [3]. Using a variability-aware compact model of HfOx-based valence-change memristors [4], we compare two circuit-level noise-injection strategies in an IMPLY gate: noise applied at the SET drive rail and noise injected through the node-resistor branch.

Our simulations show that the position of noise injection is decisive. Drive-rail noise can rescue slow switching events but also increases the risk of disturbing cells that should hold their state. In contrast, node-resistor noise is largely rejected in the hold case through the circuit's stored memristance state, while still assisting the switching case. This selective transfer widens the usable bias window and improves the correctness-versus-energy trade-off.

For the investigated gate, node-resistor noise increases the peak correctness to 98.3%, widens the usable bias window by about a factor of three, and exceeds the best noise-free operating point at approximately one fifth of its energy by enabling a shorter programming pulse. These results suggest that controlled noise, when injected at a suitable circuit node, can become a useful design resource rather than a reliability threat in memristive stateful logic.

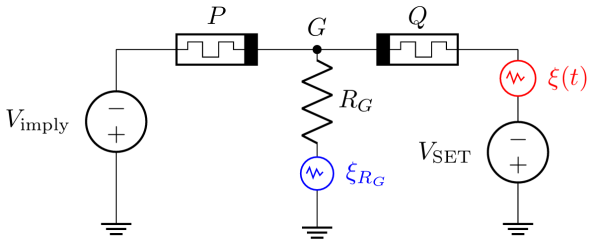


Figure 1. Memristive IMPLY gate with two possible noise-injection points. Noise can be applied either at the SET drive rail or through the node-resistor branch, leading to different transfer factors toward the switching and hold cases.

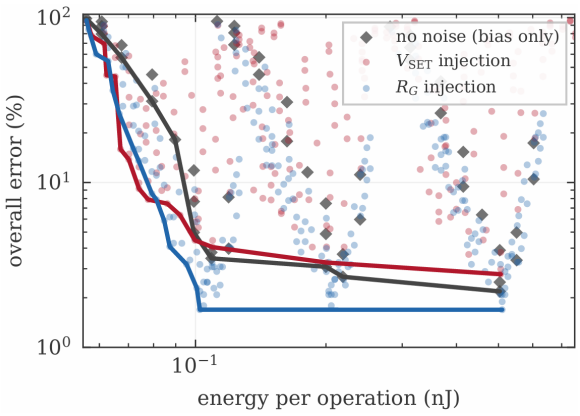


Figure 2. Overall IMPLY error versus energy per operation for noise-free operation, SET-drive noise injection, and node-resistor noise injection. Node-resistor injection provides the best high-correctness trade-off and exceeds the best noise-free point at reduced energy.

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Optimized first reset operation for more than 3-bit RRAM cells

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Although Resistive Random-Access Memory (RRAM) is a promising candidate for embedded non-volatile memory applications [1], achieving reliable multi-level cell (MLC) operations with more than 3-bit per RRAM remains challenging [2]. In particular, increasing the resistance range by programming very conductive low resistance state (LRS) levels hinders the possibility of resetting the device, degrading the capability of cycling the memory cell.

Motivated by the role of the initial reset in the conductive filament formation of the RRAM device [3], this work explores an alternative reset procedure to recover reliable programming operations while distinguishing more than 3-bit levels per cell. Specifically, a 64×64 1-transistor-1-RRAM (1T1R) array fabricated in 130 nm CMOS technology with RRAMs constituted by TiN/Ti/Al 5%: HfO_2/TiN material stack is considered [1]. MLC programming is obtained via Incremental Step Pulse Program and Verify Algorithm (ISPVA) [4], targeting eight LRS levels and one HRS.

While normal reset operations with ISPVA programming for IHP RRAM devices apply 2.3 V to the transistor gate terminal [5], the proposed alternative reset procedure, denoted as “strong reset”, employs a higher voltage signal equals to 2.5 V. After forming the whole array, the two initial reset approaches are tested on 2048 devices each. Afterwards, the same ISPVA programming procedure is employed for both groups of devices targeting identical resistance levels. Fig. 1 reports average programming success rate for each state. Noticeably, the strong reset procedure improves the switching success rate across all states, including both LRS and HRS levels. Compared to the normal approach, the new method increases the programming success rate to above 90% in nearly all cases. The only exception is the transition from LRS0 to HRS, which achieves an average success rate of approximately 84%. Nevertheless, this value remains 7% higher than that obtained using the normal approach.

In addition, to investigate if the strong initial reset has a negative impact on the long-term reliability, an endurance test comprising 1000 switching cycles is conducted on the whole array. The 1T1R cells are switched between HRS and LRS7, representing a worst-case scenario that may induce stuck-at failures. As shown in Fig. 2, devices subjected to the strong initial reset procedure exhibit a more stable switching success rate from the beginning until the end of the test. In contrast, the normal reset exhibits a lower initial success rate which gradually improves over the first 200 cycles before reaching a comparable level of performance. These results indicate that the strong reset procedure does not produce premature device failure as no evidence of degradation is observed over the course of experiment.

These results demonstrate that higher gate voltage in the first reset operation can significantly improve programming success rate and avoid any warm-up phase to stabilize the conductive filament without negatively impacting the devices’ endurance. Hence, the correct optimization of initial reset condition is a fundamental design aspect to enable 3-bit and more storage per RRAM devices.

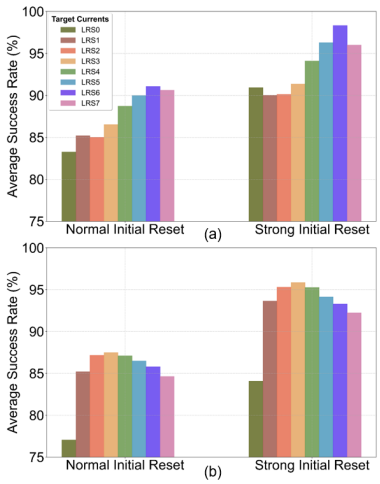


Figure 1. Average success rates in (a) the first cycle after initial reset for all considered LRSs, and in (b) the following reset procedure.

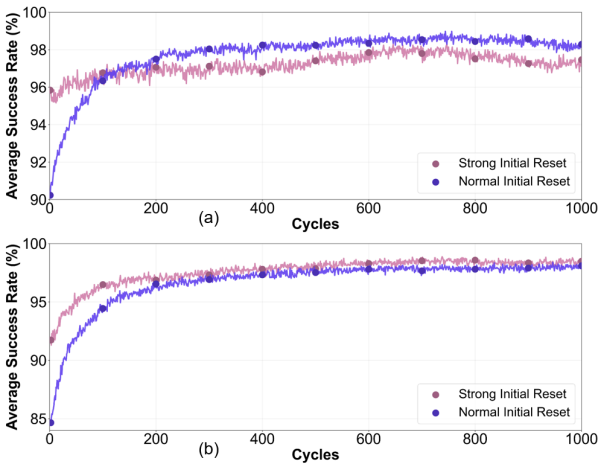


Figure 2. Average success rates across switching cycles for (a) the LRS7 state, and (b) the following reset procedure.

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Physical Verification of Memristor-based Circuits - The MACHAME Test-Chip

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Memristors, as the fourth fundamental passive circuit element, retain a programmed resistive state, offering a key building block for non-volatile (NV) analog and digital systems. This technology can strongly benefit Field-Programmable Gate Arrays (FPGAs), as more than 50% of the chip area for SRAM-based FPGAs is used for configuration memory. Compared to traditional SRAM-based memory cells, the 3D integration of memristive NV-memory using Back-End-Of-Line (BEOL) manufacturing significantly reduces the chip area needed.

To implement arbitrary digital designs, conventional FPGAs decompose logic into N-input Boolean functions stored in SRAM-backed Lookup-Tables (LUTs). In contrast, memristor-based LUTs leverage memristive voltage dividers to provide stable, static states for the memory cells. As an alternative to the multi-stage pass-transistor LUTs, a programmable logic array (PLA) inspired design utilizing crossbar-based AND/OR planes can be employed. Simulations show that this architecture is significantly more resilient to memristor defects than standard LUTs. Furthermore, replacing SRAM-backed routing multiplexers with memristive pass-gates can merge configuration memory and switching elements. These elements account for a large share of the FPGA area, as the chip-wide interconnect network connects LUTs and other elements together. Signals pass nearly unimpeded in the Low-Resistive State (LRS) and are blocked in the High-Resistive State (HRS).

The suitability of a memristive device for a given application needs to be evaluated carefully. Memristor properties depend heavily on the underlying material system, stackup and fabrication process, while performance requirements vary greatly between target applications. For the FPGA structures described above, a maximized HRS is critical to minimize quiescent leakage current, while interconnect applications require low LRS and a minimal parasitic capacitance.

Since the performance of digital test structures relies on these analog features, they need to be characterized using additional circuitry. This can allow for a more targeted approach in memristor and circuit co-design. LRS and HRS resistance, as well as cell capacitance, are expected to be key performance predictors; and depending on the application, set/reset time and error probability will further determine which circuit architecture can be chosen. The inclusion of large-scale test structures, in the form of crossbar arrays, can generate the necessary statistical data.

The MACHAME project focuses on the applied research of innovative material systems (HfOx, Y2Ox, SiC) to develop techniques for manufacturing and circuit design using memristors, integrating them with BEOL and proving the devices with test cells on real test chips. As part of this evaluation, we developed and taped out a Test-Chip in the X-Fab XT018 (180nm) process supporting programming voltages up to ±5 V. It offers top contacts for 560 memristors in total, featuring a large crossbar and dedicated test cells for FPGA structures on a 1.52×1.52mm die. The memristors are fabricated in-house at TU Darmstadt using BEOL manufacturing.

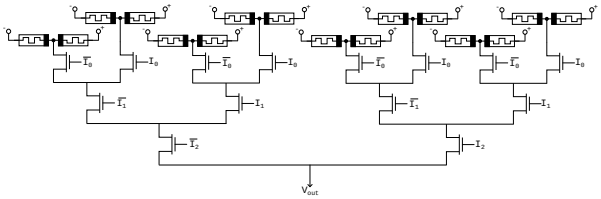


Figure 1. Circuit of a 3-Input LUT built from memristive voltage dividers

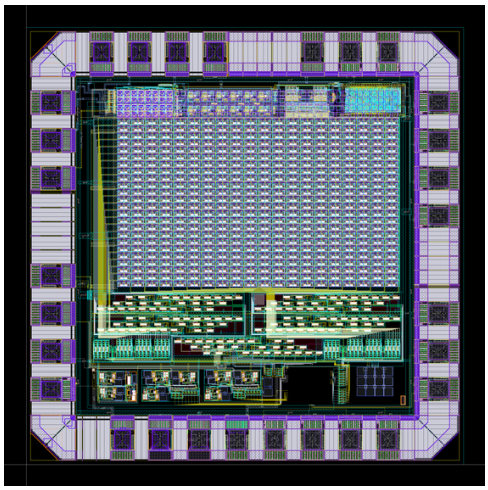


Figure 2. Layout of the Test-Chip, with large-scale test structures for analog properties in the center and FPGA test structures near the top

Pruning of ASR Models in Preparation for Efficient Crossbar Deployment

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Recent publications have shown the potential of executing non-trivial machine learning (ML) tasks on memristor crossbars via simulation. For example, [1] shows the feasibility of executing modern automatic speech recognition (ASR) on simulated memristor devices. The work uses the variability-aware vector auto-regression model Synaptogen [2] for HfO2 memristors, to map trained PyTorch ASR models onto simulated devices. The proposed SynaptogenML framework uses three concepts in order to ensure a proper mapping (cf. Fig. 1): matrix tiling, bit slicing and combination of a positive and negative bitline. This way, the influence of the device inaccuracies can be investigated on larger scale models. With the possibility to simulate larger scale networks on device, in this work we take a look at exploiting the hardware specific characteristics for the underlying neural network design. We investigate improving (theoretical) energy consumption and device count through adapted training of the ASR model. For this we focus on pruning the neural model. We identify three techniques that can be applied during training to mitigate the resulting performance degradation. 1. Structured Pruning identifies weight submatrices can be set to zero and thus omitted from the computation. Pruning submatrices the size of a crossbar array causes a significant reduction in crossbars required for the mapping, at a potential performance degradation. 2. Unstructured Pruning zeros out individual values within a vector or matrix, without enforcing structure on their position. While structured pruning usually yields efficiency improvements, unstructured pruning usually is used, for example, to reduce memory consumption [3]. In the context of memristor execution unstructured pruning can either be applied to input vector or weight matrix. A zero in the input vector (regardless of position) reduces the energy consumption of the digital-to-analog conversion of the input, while a zero weight in the weight matrix, reduces the resulting current of the operation. 3. Bit level pruning is a novel method we propose in this work. It is inspired by the combination of tiling and bit stacking used to construct the simulated crossbars. Instead of pruning a full 128x128 submatrix, we reduce the bit precision of that submatrix. This results in a substantial reduction in number of crossbars required for the construction, while retaining as much performance as possible. A visualization of the three methods can be seen in Fig. 2. In the course of our experiments, we take a look at how the ASR model can already be adapted to the pruning during training. We aim to limit the performance degradation as much as possible this way. Based on our experiments we analyze the different efficiency improvements through comparing performance degradation during deployment with efficiency improvements.

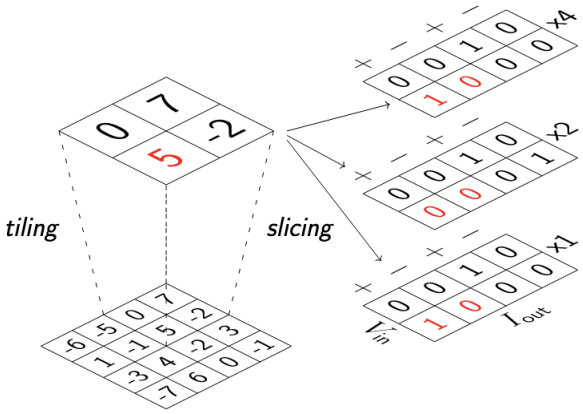


Figure 1. Exemplary mapping of a 4-bit quantized weight matrix onto 3 memristor arrays.

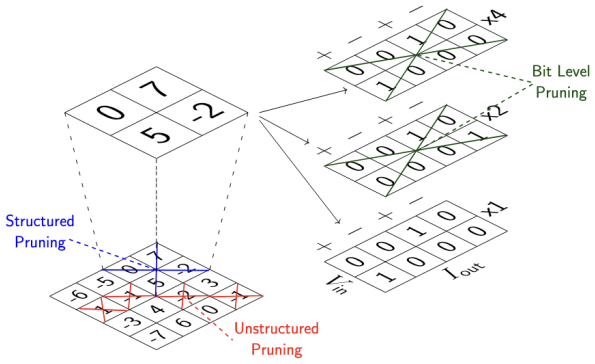


Figure 2. Exemplary application of the three different pruning methods.

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Radiation tolerance assessment of 1T1R HfO_2 memory arrays against total ionizing dose effects

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Resistive random-access memory (RRAM) is a promising candidate for non-volatile memory applications in harsh radiation environments due to its ion-based switching mechanism, unlike charge-based storage such as DRAM and Flash [1]. In addition to its radiation tolerance, HfO_2-based RRAM is compatible with CMOS fabrication processes. This allows its integration in the back-end-of-line (BEOL) to realize the 1-transistor-1-resistor (1T1R) structure, enabling multi-level programming through the precise compliance current control besides the addressing within memory arrays. However, the access transistor may become the critical vulnerability under total ionizing dose (TID) effects, motivating radiation-hardened-by-design (RHBD) solutions such as considering enclosed layout transistors (ELTs) [2].

This work presents an experimental investigation of two 9×4 1T1R RRAM arrays fabricated in IHP's 130 nm BiCMOS technology. One array employs an ELT as the access device, while the other integrates a standard high-voltage (HV) transistor, with dimensions of W = 8 µm and L = 0.66 µm, and W = 6 µm and L = 0.66 µm, respectively. Both arrays feature a BEOL integrated TiN/Al:HfO_2/Ti/TiN metal-insulator-metal (MIM) stack with 5% Al doping to improve device performance [3]. In each array, the first eight rows implement the 1T1R architecture, whereas the ninth row consists of stand-alone transistors, allowing independent evaluation of radiation-induced degradation in the access transistor. The memory cells were programmed into four resistance levels following the procedure described in [4], comprising one high-resistance state (HRS) and three low-resistance states (LRSs) (Fig. 1. b), thereby enabling 2-bit storage capability. As the structures were specifically designed for radiation characterization, no on-chip peripheral circuitry was implemented in order to isolate the failure mechanisms of the 1T1R cells. Consequently, all programming and read operations were performed using an external setup.

The arrays were exposed to X-ray irradiation up to a total accumulated dose of 1 Mrad(Si) (Fig. 1. a). During irradiation, all terminals were left floating to emulate worst case conditions, while read operations were performed every 100 krad(Si) to monitor retention characteristics. Under the same conditions, the characteristics of the transistors were measured. To further assess radiation tolerance under different ionizing radiation sources, the ELT-based array was characterized under γ-ray irradiation following the same procedure.

The results indicate a high degree of radiation tolerance for both arrays. Under X-ray irradiation no significant resistance drift was observed in the LRSs, whereas some cells programmed in the HRS exhibited resistance variations (Fig. 2). In contrast, no resistance drift was observed during the γ-ray irradiation. The ELT exhibited negligible variations in its electrical characteristics under both irradiation sources. The HV transistor also showed a high degree of radiation tolerance, although slight shifts in threshold voltage and leakage current were measured. Nevertheless, these variations remained limited and had no measurable impact on the operation of the memory array. Furthermore, the 1T1R cells could be reprogrammed and no degradation of the resistive switching parameters was observed after 1 Mrad(Si) exposure (Fig. 1. c).

This work was financially supported by the Deutsche Forschungsgemeinschaft (DFG, German Research

Foundation) under Project 551916740.

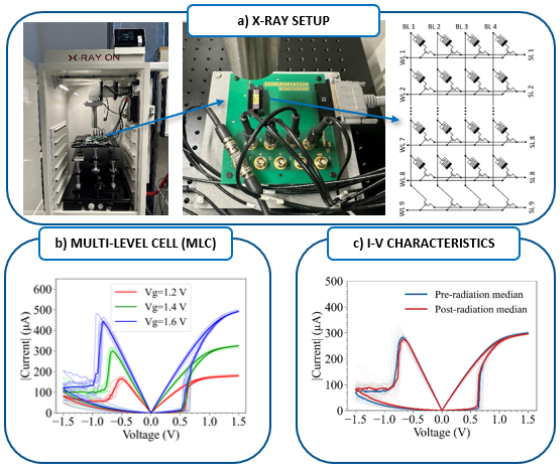


Figure 1. a) Device under test (DUT) inside the X-ray chamber. b) MLC device-to-device (D2D) current response of 32 devices under no radiation conditions. c) Comparison of current characteristics before (blue) and after (red) radiation.

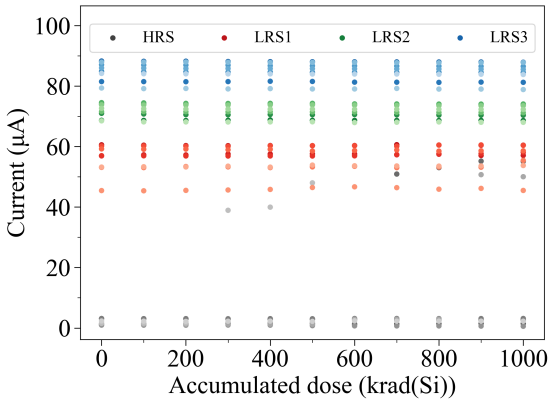


Figure 2. Readout current per memory cell measured periodically at cumulative X-ray dose steps of 100 krad(Si).

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Reduction of sneak path effects in crossbar arrays using generalized gaussian voltage signals

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This work presents a simulation study on the effects of applying generalized Gaussian voltage signals [1] to mitigate undesired programming on unselected devices in selectorless crossbar arrays caused by sneak-paths.

Crossbar arrays offer a highly dense configuration of memristive devices, serving as the core of memristor-based memories and hardware neural networks. However, they suffer from sneak-path problems during programming: unselected devices can inadvertently alter their conductance [2]. While this can be avoided by incorporating selector devices into the memory cells, such as transistors, diodes, or highly non-linear devices, it comes at the cost of increased cell complexity. Furthermore, many laboratories lack these fabrication capabilities, and commercial memristors (e.g., Knowm) are typically provided as crossbar arrays without selectors.

Several programming methodologies have been proposed to address this issue, such as applying a specific bias to unselected devices to reduce their voltage drop to 1/2 or 1/3 of the voltage applied (Vapp) to the target device [2]. Although these methods reduce the voltage stress on unselected devices, the remaining voltage can still induce unwanted conductance variations. The aim of this work is to minimize these undesired conductance changes in unselected devices under 1/2 and 1/3 bias methods by shaping the programming signals with generalized Gaussian voltage pulses [1]. The SET transition (potentiation) is investigated using the dynamic memdiode model, previously calibrated for Knowm memristors [3].

Fig. 1a shows the circuit under study, which includes a limiting series resistor. The gain factor (see Fig. 1a) is set to 1, 0.5, and 0.33 to represent the voltage on the selected device, the half-selected devices (1/2 bias schema), and the half-selected devices (1/3 bias schema), respectively. Fig. 1b illustrates the applied generalized Gaussian voltage signals and a voltage ramp of an equivalent timescale for comparison. The resulting I-V loops under ramped voltage programming are shown in Fig. 1c for the three cases. Notably, unselected devices (gain 0.5 or 0.33) undergo undesired conductance changes, which are particularly pronounced in the 1/2 bias schema.

Finally, the programming results for the different bias methods under generalized voltage signals with varying shapes (beta and sigma parameters) are shown in Figs. 2a–2c. A clear reduction in sneak-path effects is observable for specific parameter combinations, particularly for the 1/2 bias method. Since a slight reduction in the programmed value of the target device (gain = 1) also occurs in some cases, Fig. 2d plots the conductance variation relative to that of the target device as a function of the beta parameter (sigma = 0.01 s). The calculated difference in programming with generalized Gaussian signals in relation to ramped voltage stress can be attributed to the differing exposure times to the highest voltages, in addition to the non-linear dependence of the device kinetics on the voltage.

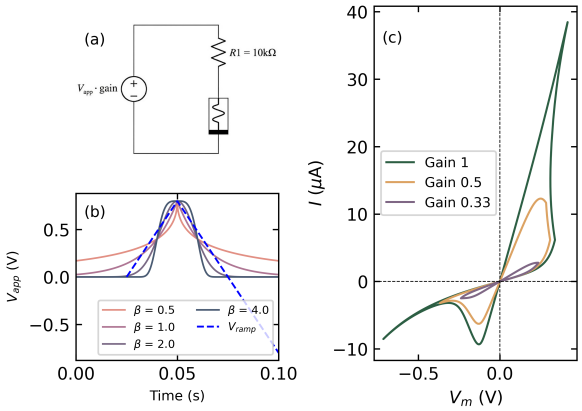


Figure 1. (a) Schematic of the circuit, consisting of a voltage source, a series resistor for current limitation and a memristor. (b) Temporal evolution of the considered generalized gaussian voltage signals for four values of the parameter beta [1] (sigma = 0.02 s). A ramped voltage signal is also shown for comparison. (c) Current versus memristor drop voltage (Vm)under the ramped voltage programming, for three different considered cases: selected device (gain 1), half-selected device with the 1/2 V bias method (gain 0.5) and half-selected device with the 1/3 V bias method (gain 0.33) [2].

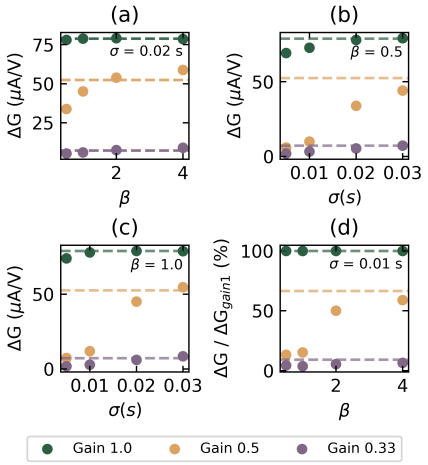


Figure 2. Conductance variation as a function of different values of the beta and sigma parameters, which determine the shape of the generalized gaussian pulses used for the device programation. Dashed lines are provided as a reference and correspond to programming using ramped voltage signals. (a)-(c) show the absolute conductance variation, while (d) represents the conductance variation in relation to the conductance variation relative to that of the target device (gain = 1).

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Reservoir Computing with Volatile Memristors for Image Recognition and Time Series Prediction

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Neural networks achieve strong performance in vision and temporal learning, but often incur high compute and energy costs due to training and data movement. Reservoir computing (RC) has emerged as an efficient alternative due to its reduced training requirements. RC consists of an input layer, a dynamical system called the reservoir, and a readout layer. Only the readout requires training, using simple linear or logistic regression algorithms. The reservoir maps input history into a high-dimensional state space through nonlinear dynamics and fading memory, and the readout produces the desired output. The reservoir can be efficiently implemented using emerging memory devices such as memristors. Memristors, particularly volatile memristors, are well suited to implement reservoirs because they exhibit nonlinear state updates under electrical stimulation and a natural decay toward equilibrium after stimulation. These intrinsic dynamics provide the nonlinearity and short-term memory required by RC, enabling compact hardware reservoirs with low training overhead.

In this work, we study a reservoir computing approach with volatile memristors called a parallel delayed feedback network (PDFN). We study methods for effectively representing the input data in the reservoir, referred to as preprocessing and encoding methods, and quantify their impact on reservoir performance, throughput, energy efficiency, and area. We analyze how practical memristor parameters, specifically state quantization, decay rate and device variability, affect reservoir performance. We study the trade-offs between these parameters and provide insights to guide design decisions. We use the MNIST image-recognition task and the nonlinear autoregressive moving average (NARMA) time-series prediction tasks as benchmarks for reservoir performance in spatial and temporal processing, respectively.

For MNIST classification, we show that informed preprocessing is crucial, and that appropriate memristor parameters such as decay rate, quantization, and input sequence length improve separability of reservoir states. We evaluate preprocessing methods including dimension, sectioning, and parity-based transformations. Sectioning improves performance by shortening the pulse sequence applied to each volatile memristor and preserving local image information, while two-dimensional and parity-based encoding enrich the reservoir representation by adding spatial and edge-like information. The optimized PDFN achieves 95.89% MNIST accuracy and remains robust under 20% device variability with accuracy up to 94.2%, showing that compact volatile-memristive reservoirs can maintain useful classification performance under practical non-idealities.

For NARMA prediction, we compare variable-frequency encoding with a variable-write-width method. The variable-write-width method preserves synchronization across reservoir branches while still producing diverse memristor responses, avoiding the alignment difficulty associated with variable-frequency operation. The results show that prediction error depends strongly on the joint choice of input encoding, decay time constant, quantization, reservoir size, training sequence length, and device variability. Higher quantization improves both accuracy and repeatability, while suitable decay dynamics and richer temporal encoding improve the reservoir representation.

Overall, the results demonstrate that volatile memristive RC performance is determined by matching the device dynamics, input representation, and reservoir architecture to the task, rather than by simply maximizing reservoir size, precision, or memory. These findings provide practical design guidance for scalable, energy-efficient memristive RC systems for temporal prediction and image recognition.

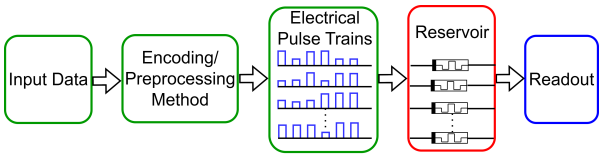


Figure 1. Generic block diagram of the memristive parallel delayed feedback network (PDFN) framework used in this work. The input data is first processed by an encoding/preprocessing method and converted into electrical pulse trains. These pulse trains are then applied to a reservoir consisting of parallel volatile memristors. The resulting read currents form the reservoir state vector, which is supplied to the readout layer to generate the output. Only the readout is trained.

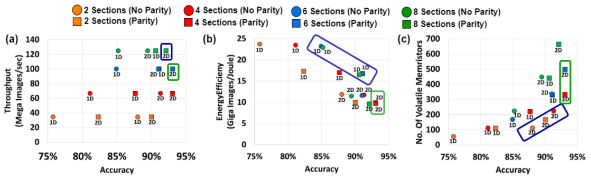


Figure 2. Trade-offs between accuracy and (a) throughput, (b) energy efficiency, and (c) area. Methods using a single section with accuracy below 75% are omitted for clarity. In (a) and (b), higher Y-axis values are better; in (c), lower Y-axis values are better. Green boxes indicate the most relevant, accurate configurations, while blue boxes highlight configurations offering a good balance between accuracy and the corresponding metric.

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RRAM-Based Multi-Context FPGA: architecture and evaluation methodology.

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Modern computing platforms range from high-performance cloud infrastructures to resource-constrained portable devices. Across this spectrum, energy-efficient hardware architectures play a crucial role. Among these, FPGAs stand out for their flexibility, enabling tailored hardware-software interaction that maximizes resource utilization [1]. However, conventional FPGAs incur substantial reconfiguration overhead, which constrains runtime adaptability and limits the frequency at which hardware resources can be dynamically shared, in contrast to CPUs and GPUs used in cloud services [2]. Multi-Context FPGAs (MC-FPGAs) address this limitation by allowing configuration changes at runtime through time-multiplexing of hardware resources without reconfiguration overhead [1] as illustrated in Fig. 1.

The increased flexibility provided by MC-FPGAs, however, requires significantly larger configuration memories and routing logic to accommodate additional contexts. This challenge motivates the exploration of emerging memory technologies that combine high storage density with CMOS compatibility, enabling efficient and scalable MC-FPGA implementations. The latter presents an opportunity to exploit the multibit storage capabilities of the Resistive Random Access Memory (RRAM), enabling multiple contexts to be stored within the same memory cell and thereby reducing area and routing overhead as illustrated in Fig. 2. Additionally, RRAMs are non-volatile memories, allowing the use of power-gating techniques to reduce energy consumption without requiring configuration reloading. Combined with their easy integration in the Back-end-of-line (BEOL)[3], these properties help reduce silicon area while increasing memory density. As a result, RRAM technology promises a significant reduction in the cost and overhead of multi-context reconfigurability, paving the way for more energy-efficient hardware architectures.

This work presents the architecture and evaluation methodology of a RRAM-based MC-FPGA. As fundamental building block of any FPGA, a novel RRAM-based Look-Up Table (LUT) component is currently under fabrication in IHP 130nm technology node [4]. The proposed design leverages multi-bit non-volatile RRAM devices to reduce the required number of memory cells while eliminating the need for external configuration memory banks. Beyond LUT implementation, RRAM devices can also be employed for the implementation of routing multiplexers (MUXs), offering similar advantages in the FPGA interconnection fabrics as reduced silicon footprint and energy-efficient non-volatile operations [5].

Functional and non-functional metrics extracted from these designs will be incorporated into system-level simulations to assess Power, Performance, and Area (PPA) characteristics of the proposed architecture, with particular emphasis on the benefits and trade-offs associated with multi-context switching. The proposed evaluation methodology leverages open-source FPGA design frameworks, including OpenFPGA [6], for netlist generation and subsequent system-level analysis. Different approaches for multi context allocation will be investigated to exploit the multi-bit storage capability of RRAM devices while ensuring reliable FPGA operation, and to assess the sharing strategies of sequential logic like Flip-Flops for an optimal PPA trade-off.

This research activity will provide valuable insights into the design of RRAM-based reconfigurable architectures and establish guidelines for efficiently integrating emerging memory technologies into future MC-FPGA platforms.

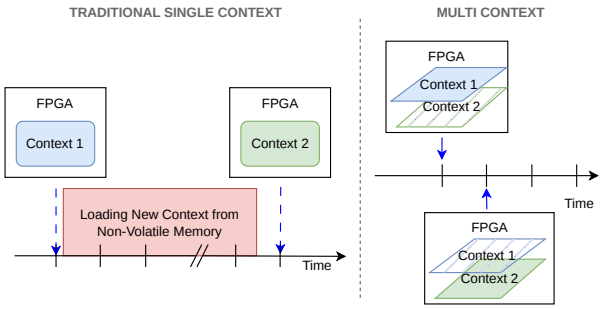


Figure 1. Illustration of mapping Logic Contexts to individual FPGA-configuration in the traditional approach (left) and the Multi Context approach (right).

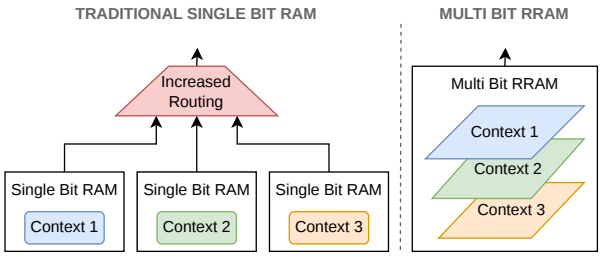


Figure 2. Illustration of Area and Routing advantages in Multi Context FPGA from Multi bit RRAM (right) over Single bit RAM (left).

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Simulation of a memristive device-based Reservoir Computing framework

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High energy consumption in artificial intelligence (AI) systems is increasingly limiting device miniaturisation, where systems with power consumption constraints like health wearables, autonomous vehicle sensors and Internet-of- Things devices must be scaled down to be marketable. Within this context, the Reservoir Computing (RC) paradigm offers a promising alternative, as the development of hardware-based RC devices could result in significant reductions in energy consumption and device footprint compared with traditional computing devices [1].

Memristive devices are two terminal electronic elements whose resistance depends on the history of applied stimuli [2]. The process is also reversible and controllable (save for device degradation and cycle-to-cycle variation), which lends itself to many interesting uses including its applications in RC and neuromorphic computing. The simulation work presented here is based on a volatile Resistive Random-Access Memory (ReRAM) device, a class of memristive device that does not retain its programmed state over time, and exhibits decaying conductance when excited. A version of the memdiode model [3] was adapted to exhibit decaying conductance states, characteristic of volatile ReRAM behaviour. Device-to-device variation and cycle-to-cycle variation are also included in the simulation. The response of the device to stimulus is used as the reservoir module, providing the non-linear dynamics and fading memory required for RC. The adaptation of the memdiode equations to demonstrate decaying conductance state widens the scope of the model and allows for the scheme's use in a broader range of neuromorphic architectures.

The architecture enables the investigation of time-series prediction and other machine learning domains in many hardware-constrained systems. Current work applies the memdiode framework to two distinct tasks, namely, handwritten digit classification (MNIST) using an RC-like model and beamtracking for 6G communications as a time-series prediction application.

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Toward Neuromorphic Hardware with Liquid Memristors: Integrating I-V based Analog Gradients and Physical Weights

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Memristor-based neuromorphic hardware holds immense promise for low-power artificial neural network implementation. However, realizing true in-situ learning remains constrained by the power-intensive circuitry required for analytical backpropagation gradients. Here, we report the implementation of an artificial neural network (ANN) with an analog gradient-based in-situ training framework instead of relying on conventional approach of using analytical gradients. Executing this architecture with liquid active layer based memristors [1] enabled low power and limited area while also harnessing the advantages of liquid devices such as low cost, simplicity, and large-scale fabrication. A hardware-in-the-loop training approach was implemented, where the intrinsic nonlinear I–V characteristics of the memristors were used as activation functions. Gradients required for backpropagation algorithm were directly obtained using an analog finite-difference method by biasing two identical devices at incrementally different voltages [2]. This enables direct computation of dI/dV without explicit modeling. The gradient extraction method showed strong similarity with the numerical gradient by achieving a mean RMSE (Root Mean Square Error) of 8.38% and high reproducibility (mean R^2 of 0.98). Using the analog gradients and leveraging the non-linearity of I-V curves, ANN simulations in Python achieved a 94.67% test accuracy on the iris dataset (5-fold Cross validation) using only two devices as neurons in a single hidden layer. This performance compares extremely well to software-based tanh activation (96%) and even outperforms ReLU activation (88.7%). Performance scalability was also demonstrated using the MNIST dataset in a two-hidden layer setup, for which a 95.9% accuracy was achieved with the devices' experimental data as hidden neurons, compared with 96.8% accuracy with tanh activation. Furthermore, when the hidden-layer weights are constrained to experimentally measured memristor conductance states the Iris network (16 devices as neurons in a single hidden layer) still achieved 90.67% test accuracy which confirms that the analog finite-difference gradient scheme is robust under realistic hardware weight quantization. These results validate the effectiveness of the analog finite-difference based gradient extraction method and highlight the potential of liquid memristor-based systems for energy-efficient neuromorphic computing.

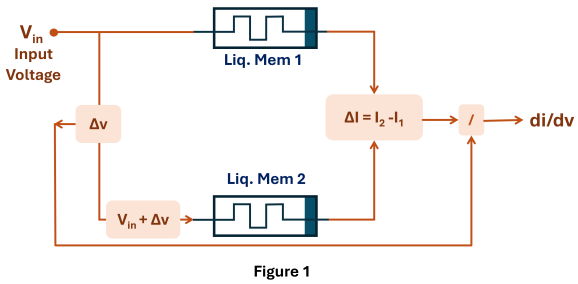


Figure 1. Schematic of the analog finite-difference gradient extraction scheme using two liquid memristor devices

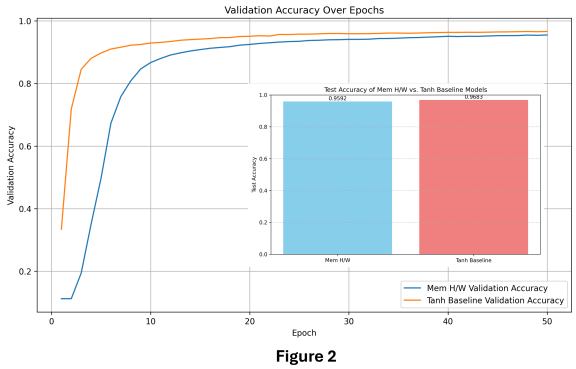


Figure 2. Validation accuracy for MNIST classification comparing liquid-memristor-based neurons with tanh activation. Inset shows final test accuracies

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Toward reliable training on highly variable memristive weights

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Memristive devices offer a promising route toward energy-efficient neural network implementations, however, their intrinsic stochasticity poses a major obstacle to reliable learning. Conventional methods for deep neural networks training, such as stochastic gradient descent are highly sensitive to the inaccuracies in conductance updates, resulting in a pronounced spread in classification accuracy. To address this limitation, we introduced a combination of random coordinate descent and a learning-from-mistakes strategy, which localizes weight updates and avoids unnecessary conductance changes. Simulations show that conventional stochastic gradient descent exhibits substantial accuracy variability (5%), while the proposed approach reduces this spread to 0.1% and maintains peak performance for MNIST handwritten digits dataset. Additionaly, experimental validation on a HfO2-based 1T1R RRAM crossbar array confirms the feasibility of the method and strong agreement between simulation and hardware results. The proposed training framework provides a scalable pathway toward robust learning in memristive neuromorphic systems.

Towards Design of Bio-realistic third-order Memristive Neuron Circuits for Neuromorphic Computing

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As conventional computing architectures approach fundamental limits imposed by device scaling and the von Neumann bottleneck, neuromorphic computing has gained increased attention inspired by the remarkable computational and energy efficiency of biological neural systems across diverse cognitive tasks where computation emerges from continuous nonlinear dynamics and event-driven spiking activity. Biological neurons are inherently nonlinear dynamical systems that exhibit a wide range of behaviors, which are captured well by computational neuron models. Locally active memristors (LAMs) that exhibit negative differential resistance (NDR) enable natural hardware implementation of neuronal dynamics. While exhibiting various spiking patterns, existing designs of memristor-based neuron circuits [1-3] are dynamically different from their biological counterparts, as is evident from their subthreshold dynamics and spike waveforms. Furthermore, neuron-like behaviors are often demonstrated through empirical parameter tuning, lacking a clear connection to biological models.

In this work, we develop a principled bottom-up approach for the design of bio-realistic third-order memristor-based neuron circuits, through a dynamical systems framework based on phase flow analysis and bifurcation diagrams. We begin with the standard second-order LAM neuron circuit [4] and show that replacing the linear bias resistor with a nonlinear resistor exhibiting diode-like characteristics R_exp (circuit illustrated in Fig. 1(a)) reproduces bio-plausible nullclines and dynamics. Through extensive bifurcation analysis as depicted in Fig. 1(b), we identify five operating regions, including two novel bistable regimes B1 and B2 which arise from a series of co-existing saddle-node and supercritical Hopf bifurcations. Regime B1 contains a bistability between two stable fixed points, whereas B2 contains coexistence of a stable fixed point and a limit cycle, enabling switching via initial conditions or transient pulses between UP/DOWN states in B1 and between quiescence and spiking in B2. To the best of our knowledge, such a rich bifurcation structure has not been demonstrated in a physically grounded electrical neuron circuit before.

Furthermore, this second-order system is then extended to a third-order memristive neuron circuit where the bistable regimes B1 and B2 are exploited to exhibit bursting and adaptation dynamics through fast-slow decomposition. The third state variable 'x' is introduced by incorporating threshold-based slow dynamics into the nonlinear resistor, transforming it into a nonlinear memristive element. Fig. 2 depicts the bursting dynamics exhibited by our system. Thus, the third-order system arises from slow modulation of the second-order dynamics, analogous to fast–slow biological neuron models. It is important to note that the circuit function is agnostic to the exact form of the modulation. We analyze the bursting mechanism and show that it corresponds to Hopf/Fold geometry of bursting (Fig. 2). Finally, we analyze the I-V characteristics of the nonlinear memristor to ensure that it is physically grounded and show that it features volatile inverse hysteresis characteristics similar to that of the biological potassium ion channel [5]. This highlights the importance of inverse hysteresis as a key device property for constructing memristive neuron circuits that are truly analogous to biological neuron models, offering new opportunities and motivation for engineering of such devices.

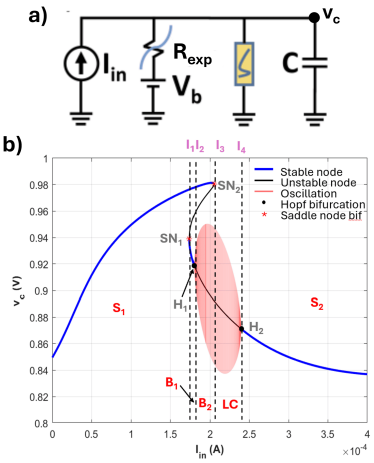


Figure 1. (a) LAM-based neuron circuit with diode-like nonlinear bias resistor R_exp. (b) Bifurcation diagram corresponding to the state v_c of the LAM neuron. I_in is the bifurcation parameter. Stable and unstable equilibrium points are denoted by blue and black lines respectively. There are five different dynamical regimes in the system, separated by black dotted lines for visual clarity and labeled S_1, B_1, B_2, LC, S_2. The bifurcation points are labeled in gray characters, H_i for Hopf and SN_i for Saddle-node bifurcations.

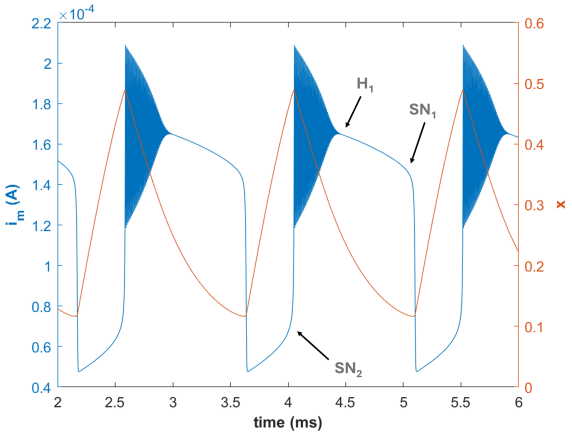


Figure 2. Bursting dynamics of the third-order neuron circuit with slow-fast structure, it is evident that the third state variable "x" modulates the excitability of the fast subsystem. H1, SN1 and SN2 are the dynamical bifurcations involved in the bursting mechanism.

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Trade-Offs Between Volatile and Non-Volatile Memristors for RF Switching Applications

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Radiofrequency (RF) switches are essential components in modern wireless communication systems, enabling signal routing, antenna selection, and reconfigurable front-end architectures. Future communication networks require switching devices that combine low power consumption with high-frequency operation. Memristive devices have emerged as promising candidates for RF switching applications owing to their nanoscale dimensions, programmable resistance states, and potential for low-power reconfigurable hardware [1]. Depending on their switching behaviour, memristors can be broadly classified into volatile and non-volatile types. Volatile memristors exhibit bias-triggered temporary switching, making them attractive for dynamically reconfigurable RF systems, whereas non-volatile memristors retain their resistance states after the external bias is removed, enabling persistent configuration without static power consumption. Despite these distinct operating mechanisms, their relative RF characteristics and application suitability have not been systematically compared.

In this work, a volatile niobium oxide (NbOx) memristor and a non-volatile hafnium oxide (HfO2) memristor were implemented as RF switching elements using physics-based LTspice models [2-4]. Equivalent RF switch circuits were developed and characterized through S-parameter analysis over the frequency range from 1 MHz to 40 GHz. The volatile NbOx memristor exhibited efficient RF transmission characteristics with an insertion loss of 4 dB in the ON state and an ON/OFF transmission contrast of approximately 17 dB. In contrast, the non-volatile HfO2 memristor achieved a larger ON/OFF transmission contrast of approximately 26 dB and a significantly higher OFF-state isolation of −57 dB, while maintaining the programmed resistance state without continuous bias. The NbOx device also exhibited improved impedance matching in the ON state, with S11 approaching −9 dB.

The results reveal a fundamental trade-off between volatile and non-volatile switching mechanisms that leads to distinct RF behaviors. The volatile NbOx memristor favors threshold-triggered and dynamically reconfigurable operation with improved signal transmission, whereas the non-volatile HfO2 memristor provides superior isolation and state retention, making it attractive for energy-efficient and state-retentive RF front-end architectures.

Building upon these initial results, ongoing work focuses on investigating how key model parameters influence the RF performance of both volatile and non-volatile memristors, with particular emphasis on their impact on insertion loss, isolation, and switching characteristics. The study is also being extended to additional material systems, including volatile VO2 and V3O5 devices and non-volatile TiO2 and Ta2O5 memristors, to enable a broader comparison across different switching mechanisms and to establish a unified framework for evaluating memristive RF switches. These findings provide insights into the advantages and limitations of different memristive switching classes and offer guidance for selecting suitable devices for future reconfigurable RF systems.

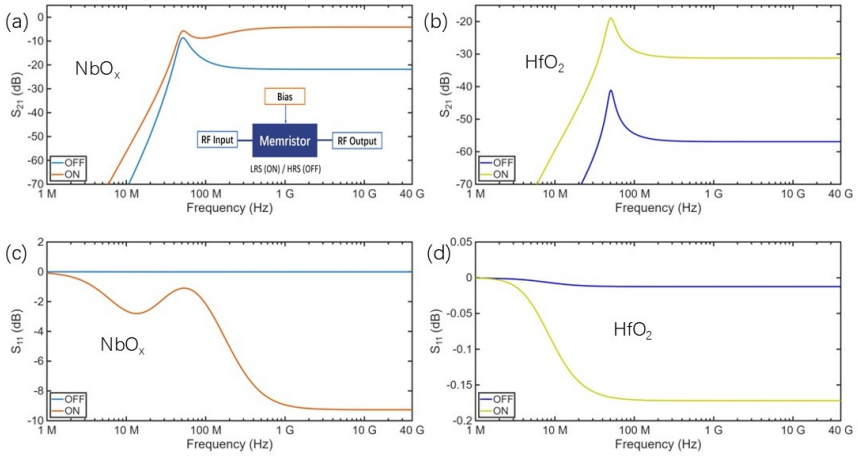


Figure 1. (a) S21 of NbOx volatile memristor RF switch with schematic of the structure (b) S21 of HfO2 non-volatile memristor RF switch (c) S11 of NbOx volatile memristor RF switch (d) S11 of HfO2 non-volatile memristor RF switch

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